

Packet Speech Program Review Meeting

June 3, 1982

**Sponsored By
Department of Defense
Defense Advanced Research Projects Agency**

**Hosted By
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY**

Foreword

The Defense Advanced Research Projects Agency sponsored a meeting on June 3, 1982, at Lincoln Laboratory to review the results of the DARPA Packet Speech Program and to demonstrate packet speech technology to a group of invited visitors from the Department of Defense. The purpose of this document is to record the proceedings of the meeting by collecting the visual aids used in the technical presentations and in the demonstration.

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 Information Sciences Institute
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 Clifford J. Weinstein, MIT Lincoln Laboratory
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AGENDA FOR DARPA PACKET SPEECH MEETING

Lincoln Laboratory

3 June 1982

<u>TIME</u>	<u>TOPIC</u>	<u>SPEAKER</u>
0930-1100	Background, Goals, Key Results, and Demo	Adams (DARPA)
1100-1115	Break	
1115-1135	Network Voice Protocols	Cohen (ISI)
1135-1150	Speech Conferencing	Forgie (Lincoln)
1150-1205	Wideband Network	Weinstein (Lincoln)
1205-1225	Packet Radio Speech	Craighill (SRI)
1230-1330	Lunch	
1330-1350	Summary of Key Algorithm Developments	Makhoul (BBN)
1350-1405	Very Low-Rate Speech	Schwartz (BBN)
1405-1425	Packet Voice Terminal	O'Leary (Lincoln)
1425-1445	Break	
1445-1500	Compact LPC Vocoder	Feldman (Lincoln)
1500-1515	Flexible Array Processor	Culler (CHI Systems)
1515-1530	VLSI Array Processor	Greenwood (Motorola)
1530-1545	Single Chip LPC	Brodersen (U.C. Berkeley)
1545-1630	Future Plans and Discussion	Kahn (DARPA)

Attendees

<u>Name</u>	<u>Affiliation</u>
Abene, Capt. Peter	DCA
Adams, Lt. Col. Duane	DARPA/IPTO
Barna, Joseph	DCEC
Beauchemin, Edward	MIT-LL
Berger, Robert	MIT-LL
Bially, Ted	MIT-LL
Blankenship, Peter	MIT-LL
Blumenthal, Steven	BBN
Brodersen, Robert	U. California/Berkeley
Burchfiel, Jerry	BBN
Casner, Stephen	ISI
Cohen, Dan	ISI
Cole, Randy	ISI
Cowles, Jack	Western Union
Craighill, Earl	SRI International
Crawford, Richard	DCA
Culler, Glen	CHI Systems, Inc
Deckelman, Francis	NAVELEX
Falk, Gilbert	BBN
Falk, Col. Harold	ESD
Feldman, Joel	MIT-LL
Forgie, James	MIT-LL
Forsdick, Harry	BBN
Friedhoffer, Carol	NSA
Fussell, Jesse	NSA
Gilbert, Warren	ESD
Glazim, Bernard	Western Union
Gold, Bernard	MIT-LL
Greenwood, Edward	Motorola
Heggestad, Harold	MIT-LL
Hoversten, Estil	Linkabit
Johnson, Robin	OSD
Kahn, Robert	DARPA
Kang, George	NRL
Kantrowitz, William	MIT-LL
Kline, Lee	NRL
Krasner, Michael	BBN

Lippmann, Richard
Luksevicius, Albinas
Lynn, Verne L.

Makhoul, John
McCammon, Michael
McElwain, Constance
McLaughlin, Alan
Moran, George
Morris, Paul
Morrow, Walter

Northrup, Richard

O'Leary, Gerald

Parker, James
Paul, Douglas
Peatfield, C. Ross
Peeler, Charles
Proctor, William

Rettberg, Randy
Roucos, Salim

Sandy, G. Ferrell
Schechter, Harold
Schwartz, Perry
Schwartz, Richard
Secrest, Bruce
Segota, Anton
Sharpe, Lt. Grady
Shippee, Bernard
Sonini, Lt. Col. Joseph
Sues, Larry

Taylor, Lee
Thomas, Robert
Tierney, Joseph
Tomlinson, Raymond
Tremain, Thomas

Viswanathan, Vishu

Weinstein, Clifford

Zimmermann, Lt. Col. Frank

MIT-LL
Ft. Monmouth
DARPA

BBN
CHI Systems, Inc.
MIT-LL
MIT-LL
DCEC
Ft. Monmouth
MIT-LL

RADC

MIT-LL

MITRE
MIT-LL
MIT-LL
Ft. Bragg
CHI Systems, Inc.

BBN
BBN

MITRE
ESD
MITRE
BBN
Texas Instruments, Inc.
ESD
ESD
Western Union
ESD
RADC

MIT-LL
BBN
MIT-LL
BBN
NSA

BBN

MIT-LL

DCEC

Organization Addresses

BBN

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50 Moulton Street
Cambridge, MA 02138

CHI Systems, Inc.

CHI Systems, Inc.
150-A Aero Camino
Goleta, CA 93017

DARPA

DARPA/IPTO
Architect Building
1400 Wilson Boulevard
Arlington, VA 22209

DCA

Defense Communications Agency
4135 Courthouse Road
Arlington, VA 22209

DCEC

Defense Communications Engineering Center
1860 Wiehle Avenue
Reston, VA 22090

ESD

Electronic Systems Division
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Bedford, MA 01731

FT. BRAGG

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Fort Bragg, NC 28307

FT. MONMOUTH

Hqs., U. S. Army
Communications Electronics Command
Ft. Monmouth, NJ 07703

ISI

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4676 Admiralty Way
Marina Del Rey, CA 90291

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10453 Roselle Street
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MIT-LL
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P. O. Box 73
Lexington, MA 02173

MITRE
MITRE Corporation
Bedford, MA 01731

Motorola
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Government Electronics Division
8201 E. McDowell Road
Scottsdale, AZ 85251

NAVELEX
Naval Electronics Command
Washington, D.C. 20366

NRL
Naval Research Laboratory
4555 Overlook Avenue, SW
Washington, D.C. 20375

NSA
Director
National Security Agency
9800 Savage Road
Ft. George G. Meade, MD 20755

OSD
Office Secretary of Defense
Washington, D.C. 20301

RADC
Rome Air Development Center
Griffiss AFB, NY 13441

SRI
SRI International
333 Ravenswood Avenue
Menlo Park, CA 94025

Texas Instruments, Inc.
P. O. Box 225936
Dallas, TX 75265

U. of California
U. of California/Berkeley
Dept. of EE/CS
Cory Hall
Berkeley, CA 94720

WU
Western Union
One Lake Street
Upper Saddle River, NJ 07458

PACKETIZED SPEECH OVERVIEW

3 JUNE 1982

LT. COL. DUANE A. ADAMS
DARPA

PACKETIZED SPEECH

OBJECTIVES

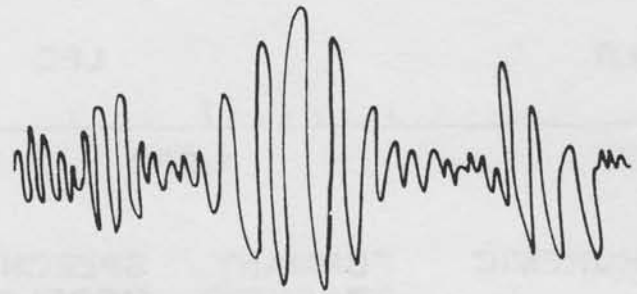
- **ACHIEVE POINT-TO-POINT AND CONFERENCED NARROWBAND DIGITAL SPEECH THROUGH PACKET-SWITCHED NETWORKS**
- **DEVELOP ALGORITHMS FOR DEGRADED SPEECH ENVIRONMENTS**
- **DEMONSTRATE MULTI-USER INTEGRATED DATA/VOICE TRANSMISSIONS**
- **MAINTAIN COMPATIBILITY WITH END-TO-END SECURITY AND INTERNET PROTOCOLS**
- **DEVELOP LOW-COST PACKET SPEECH HARDWARE**

PACKETIZED SPEECH

MAJOR THRUSTS

- ALGORITHMS
- NETWORKS
- HARDWARE

PACKETIZED SPEECH



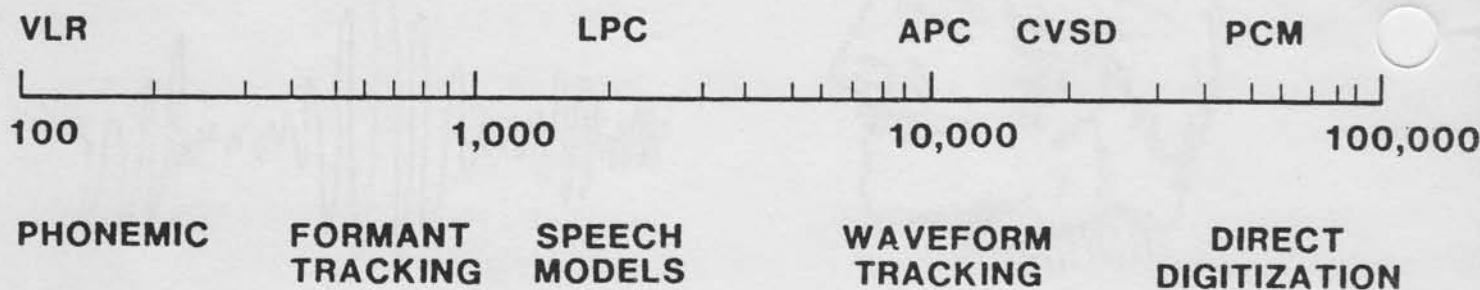
TIME

SPEECH FREQUENCY RANGE: 0-4000 Hz

SAMPLING FREQUENCY: 8000 SAMPLES/SEC

PCM DATA RATE: 64,000 BITS/SEC

PACKETIZED SPEECH



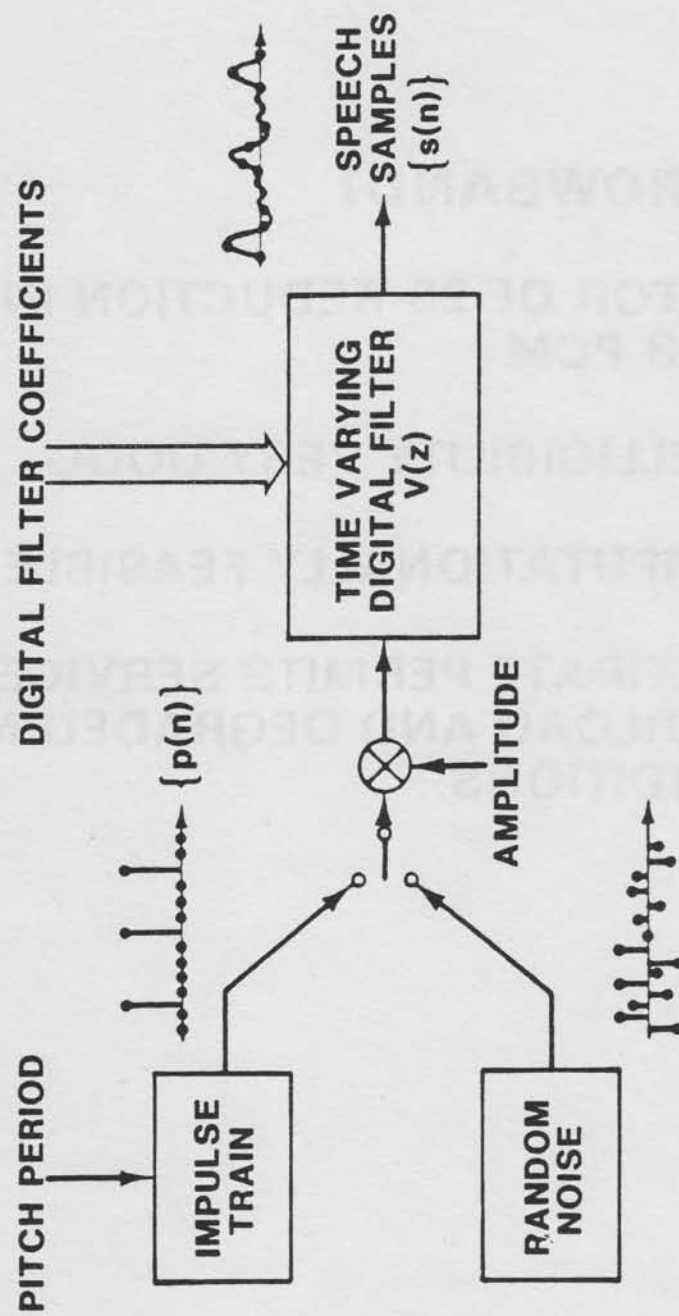
DIGITAL SPEECH REPRESENTATIONS

PACKETIZED SPEECH

WHY NARROWBAND?

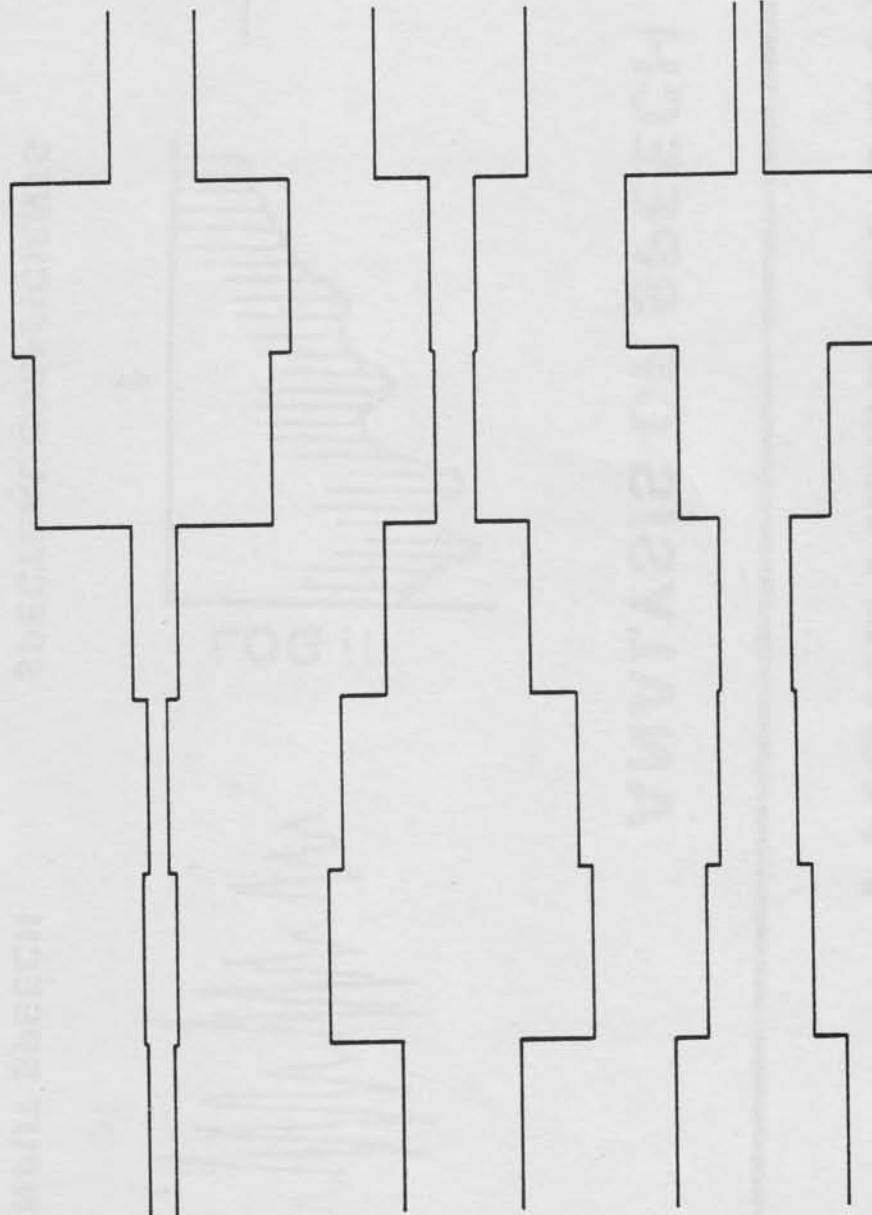
- FACTOR OF 25 REDUCTION IN BANDWIDTH OVER PCM
- INTELLIGIBILITY VERY GOOD
- COMPUTATIONALLY FEASIBLE
- MULTIRATE PERMITS SERVICE UNDER OVERLOAD AND DEGRADED NETWORK CONDITIONS

PACKETIZED SPEECH



SPEECH PRODUCTION MODEL

PACKETIZED SPEECH



a AS IN FATHER

e AS IN BEAT

o AS IN BOAT

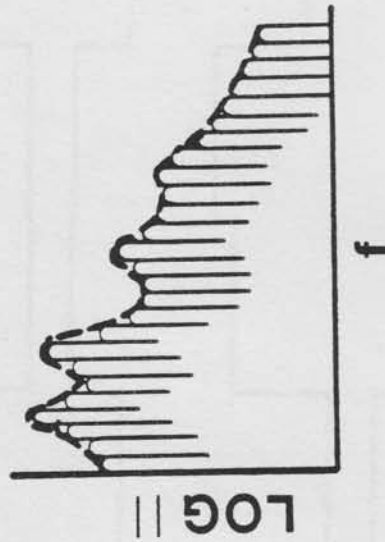
VOCAL TRACT MODEL FOR 3 VOWELS

PACKETIZED SPEECH

ANALYSIS OF SPEECH



INPUT SPEECH



SPECTRAL COEFFICIENTS



PITCH

$T = 10$ TO 20 msec, 150 SAMPLES OF SPEECH
SPEECH ASSUMED TO BE STATIONARY OVER T

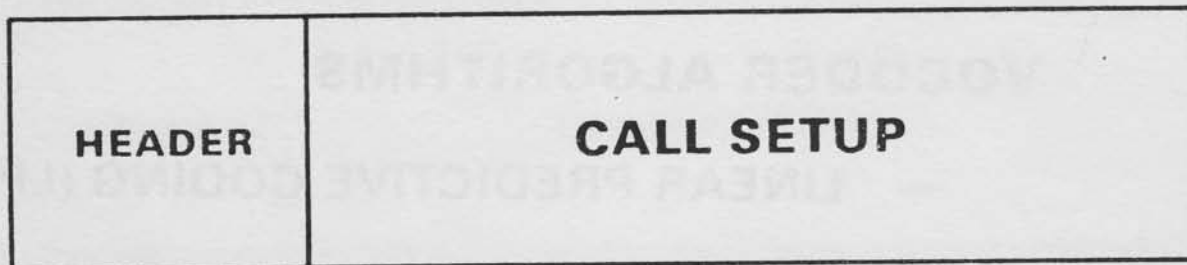
PACKETIZED SPEECH

VOCODER ALGORITHMS

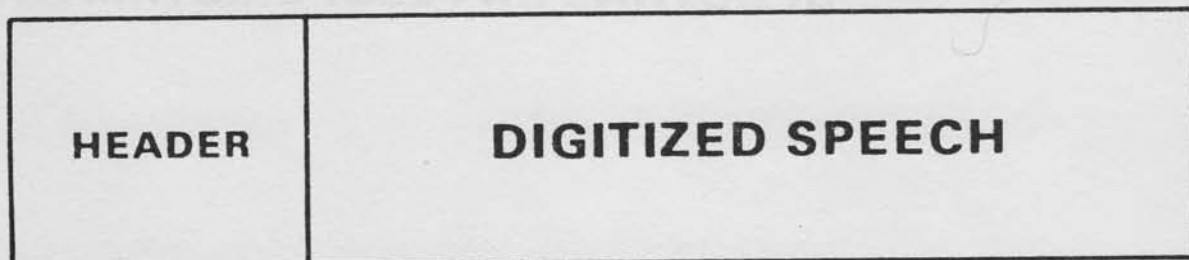
- **LINEAR PREDICTIVE CODING (LPC)**
- **CHANNEL VOCODER**
- **HOMOMORPHIC VOCODER**
- **SPECTRAL ENVELOPE ESTIMATION**

PACKETIZED SPEECH

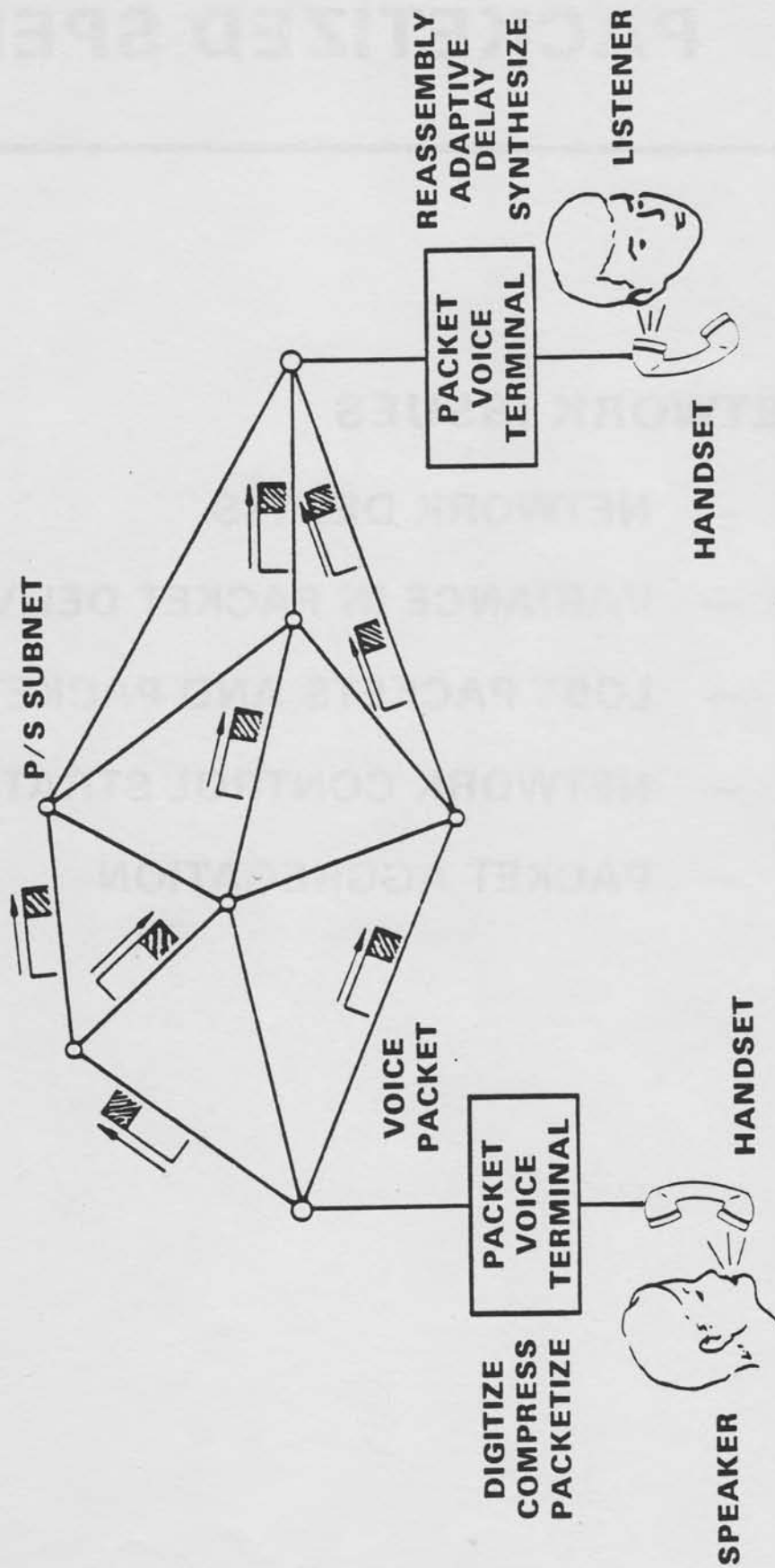
CONTROL PACKETS



DATA PACKETS



PACKETIZED SPEECH



PACKET VOICE/DATA NETWORK

PACKETIZED SPEECH

NETWORK ISSUES

- NETWORK DELAYS
- VARIANCE IN PACKET DELIVERY
- LOST PACKETS AND PACKET REASSEMBLY
- NETWORK CONTROL STRATEGIES
- PACKET AGGREGATION

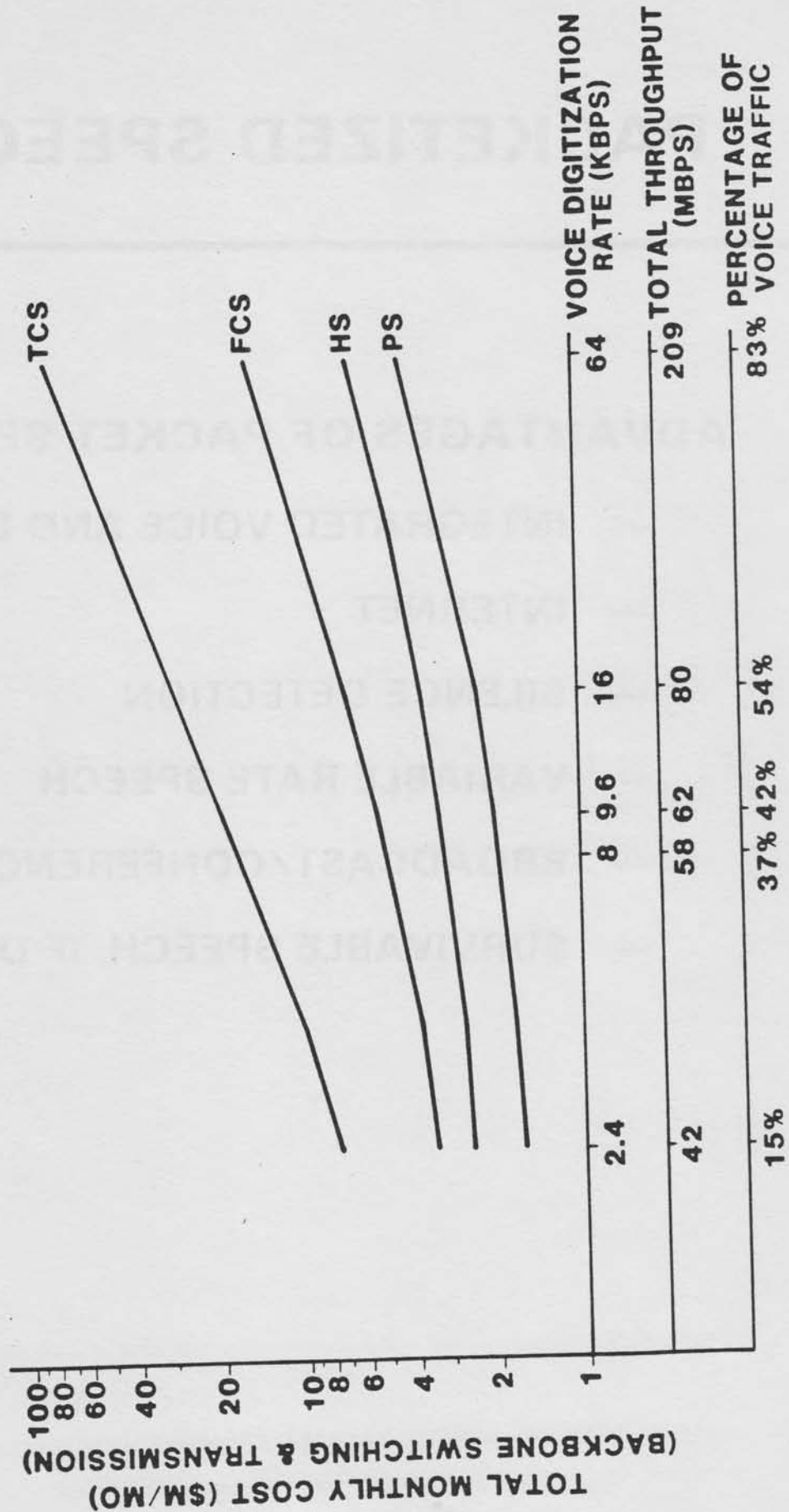
PACKETIZED SPEECH

ADVANTAGES OF PACKET SPEECH

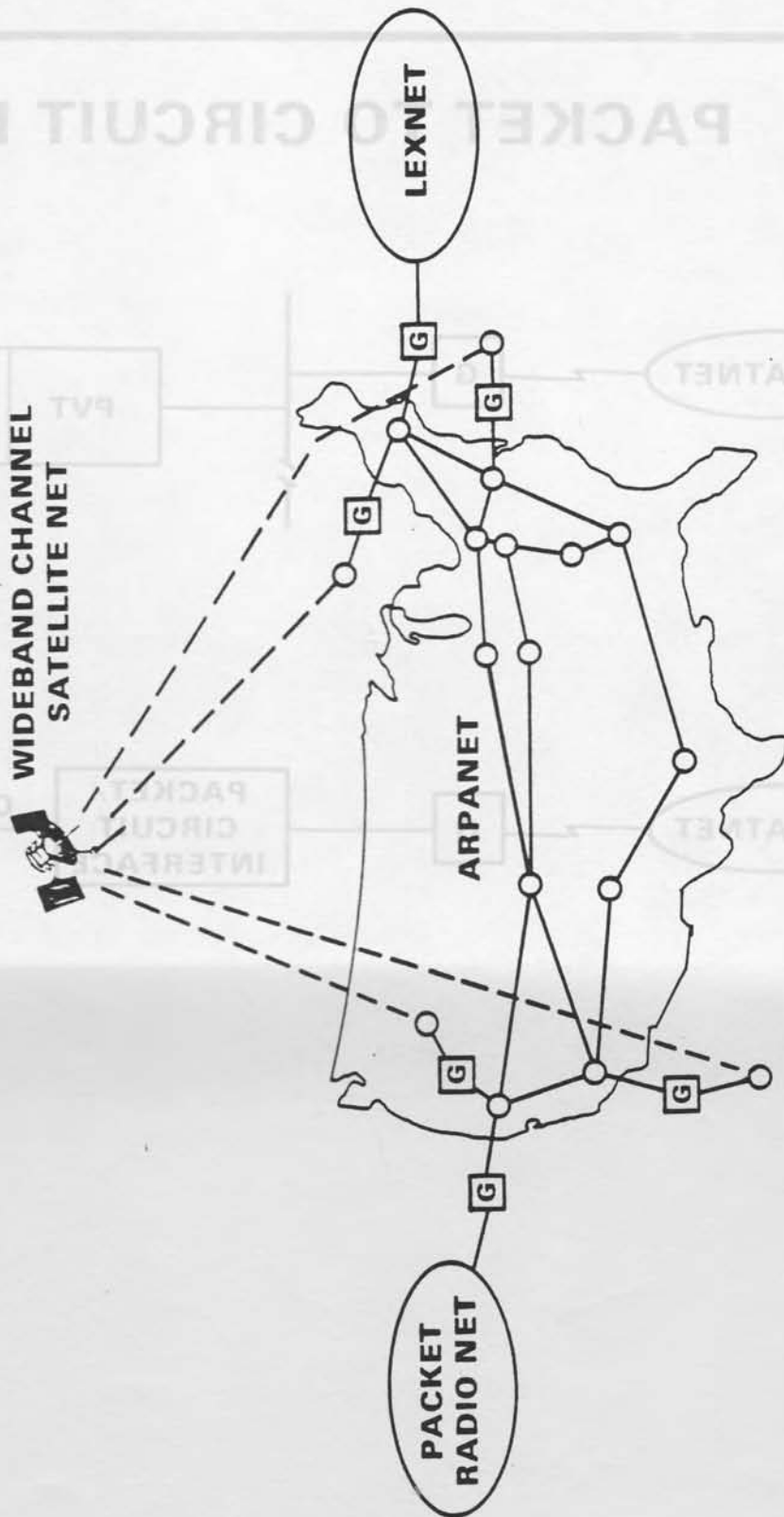
- INTEGRATED VOICE AND DATA
- INTERNET
- SILENCE DETECTION
- VARIABLE RATE SPEECH
- BROADCAST/CONFERENCING
- SURVIVABLE SPEECH, IF DESIRED

PACKETIZED SPEECH

TRAFFIC: 2,700 ERLANGS VOICE TRAFFIC
36.15 MBPS DATA TRAFFIC



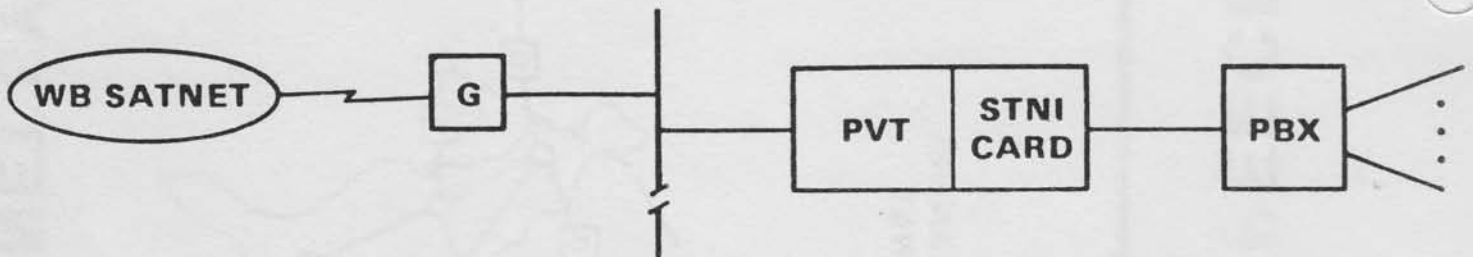
PACKETIZED SPEECH



EXPERIMENTAL INTERNET SYSTEM

PACKETIZED SPEECH

PACKET TO CIRCUIT INTERFACE



PACKETIZED SPEECH

MAJOR MILESTONES

1974 CVSD DEMONSTRATED ON ARPANET

LPC DEMONSTRATED ON ARPANET

NVP PROTOCOLS DEVELOPED

1976 LPC CONFERENCE ON ARPANET

1977 VARIABLE FRAME RATE LPC

PACKETIZED SPEECH

MAJOR MILESTONES (CONT.)

- 1978** CVSD DEMONSTRATED ON PACKET RADIO NET
SATNET CONFERENCING WITH LPC
SPECTRAL ENVELOPE ESTIMATION ALGORITHM
- 1979** REAL-TIME VARIABLE RATE CHANNEL VOCODER
INTERNET SPEECH DEMONSTRATED
- 1980** VOICE TERMINAL DEMONSTRATED ON LOCAL NET

PACKETIZED SPEECH

MAJOR MILESTONES (CONT.)

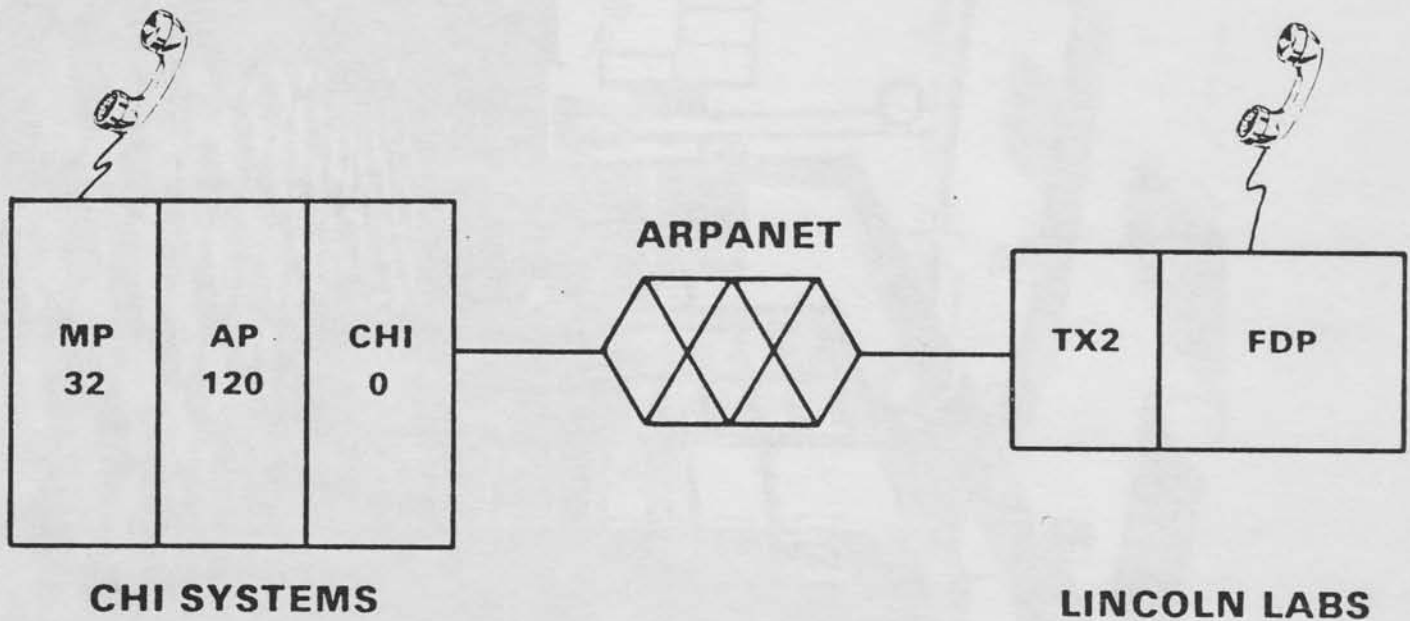
1981 **NVP-II/ST PROTOCOLS**
CHI-5 ARRAY PROCESSOR DEVELOPED
LPC SPEECH ON PACKET RADIO NET
PCM ON WIDEBAND CHANNEL

PACKETIZED SPEECH

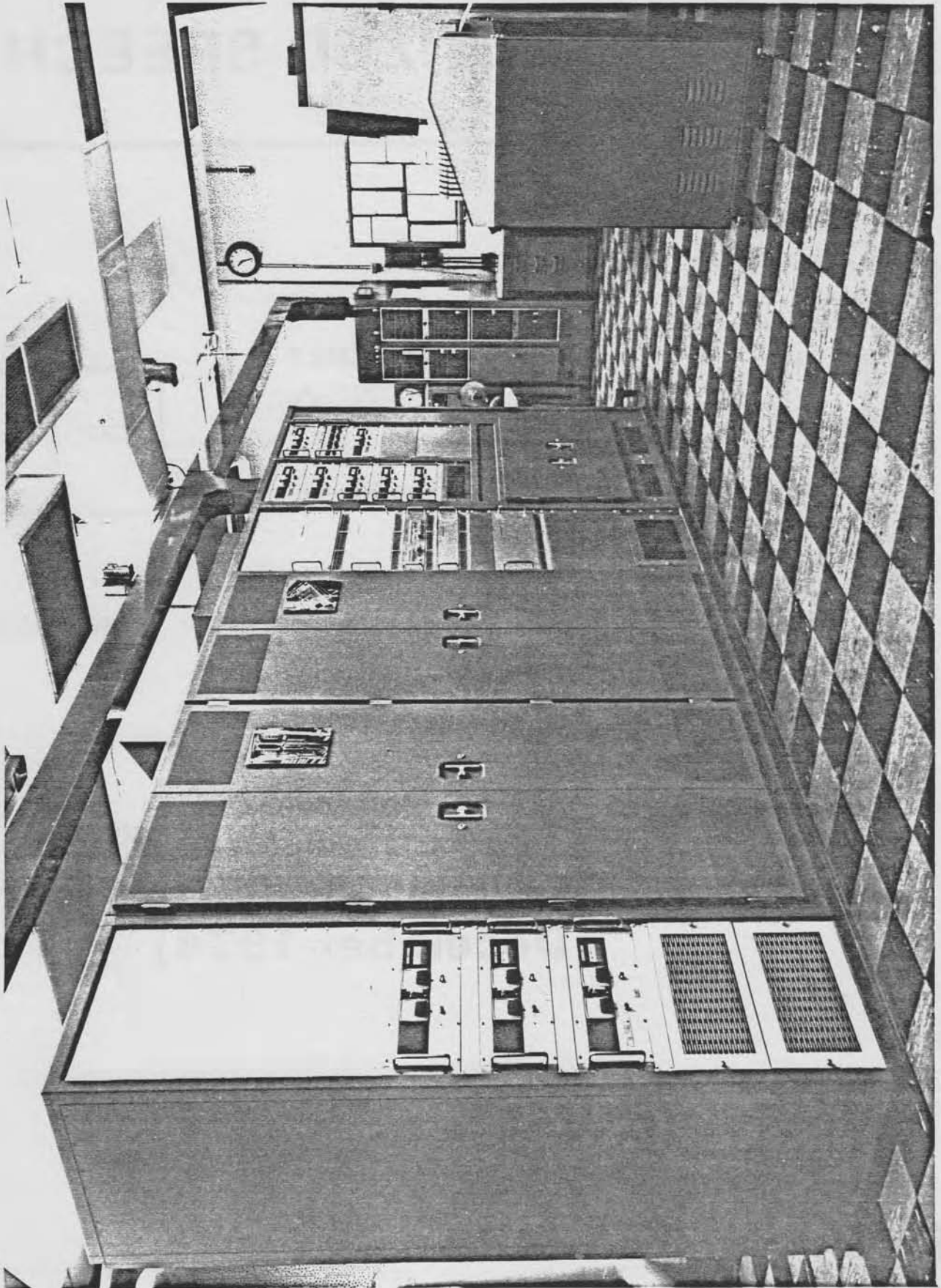
MAJOR MILESTONES (CONT.)

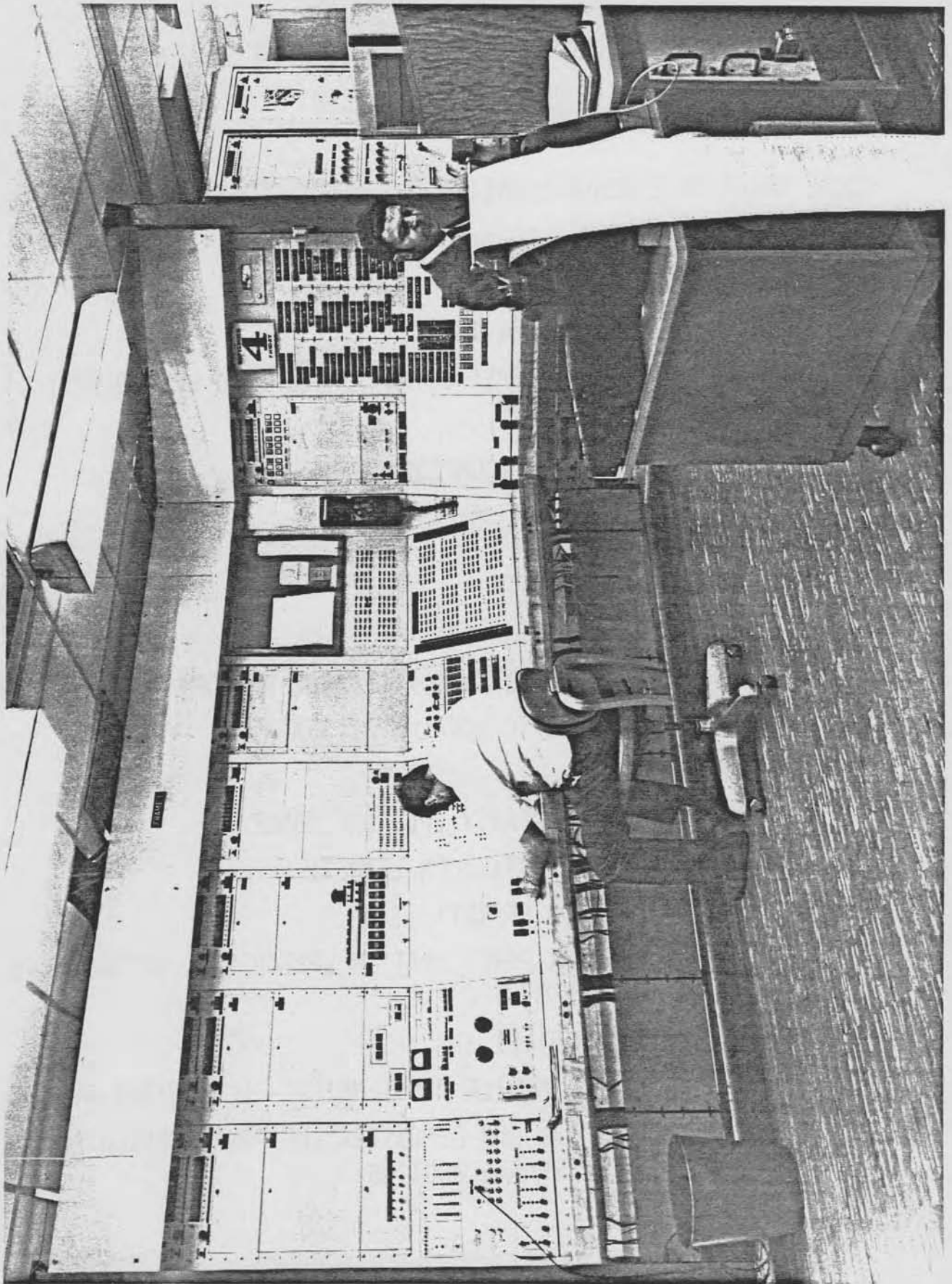
1982 **COMPACT LPC VOCODER (NEC)**
LPC ON WIDEBAND NETWORK
MULTI-RATE SPEECH ON WIDEBAND
(PCM AND CVSD)
INTERNET CONFERENCING
MOBILE LPC ON PACKET RADIO NET

PACKETIZED SPEECH



**INITIAL NETWORK LPC
DEMONSTRATION
(December 1974)**





SUMMARY OF
PACKET SPEECH DEMONSTRATION SEQUENCE
JUNE 3, 1982

LOCAL CALLS ON LINCOLN LEXNET

POINT-TO-POINT

1. PCM (64 KBPS)
2. ECVSD (16-64 KBPS)
3. LPC (2.4 KBPS) USING SINGLE-CARD LPC IN PVT)

CONFERENCE

4. PCM 4-PARTY CONFERENCE

CALLS OVER WIDEBAND SATNET

POINT-TO-POINT

5. PCM LL - ISI
6. PCM LL - SWITCHED TELEPHONE NETWORK INTERFACE AT ISI
(CALL TO LOCAL L.A. WEATHER)

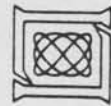
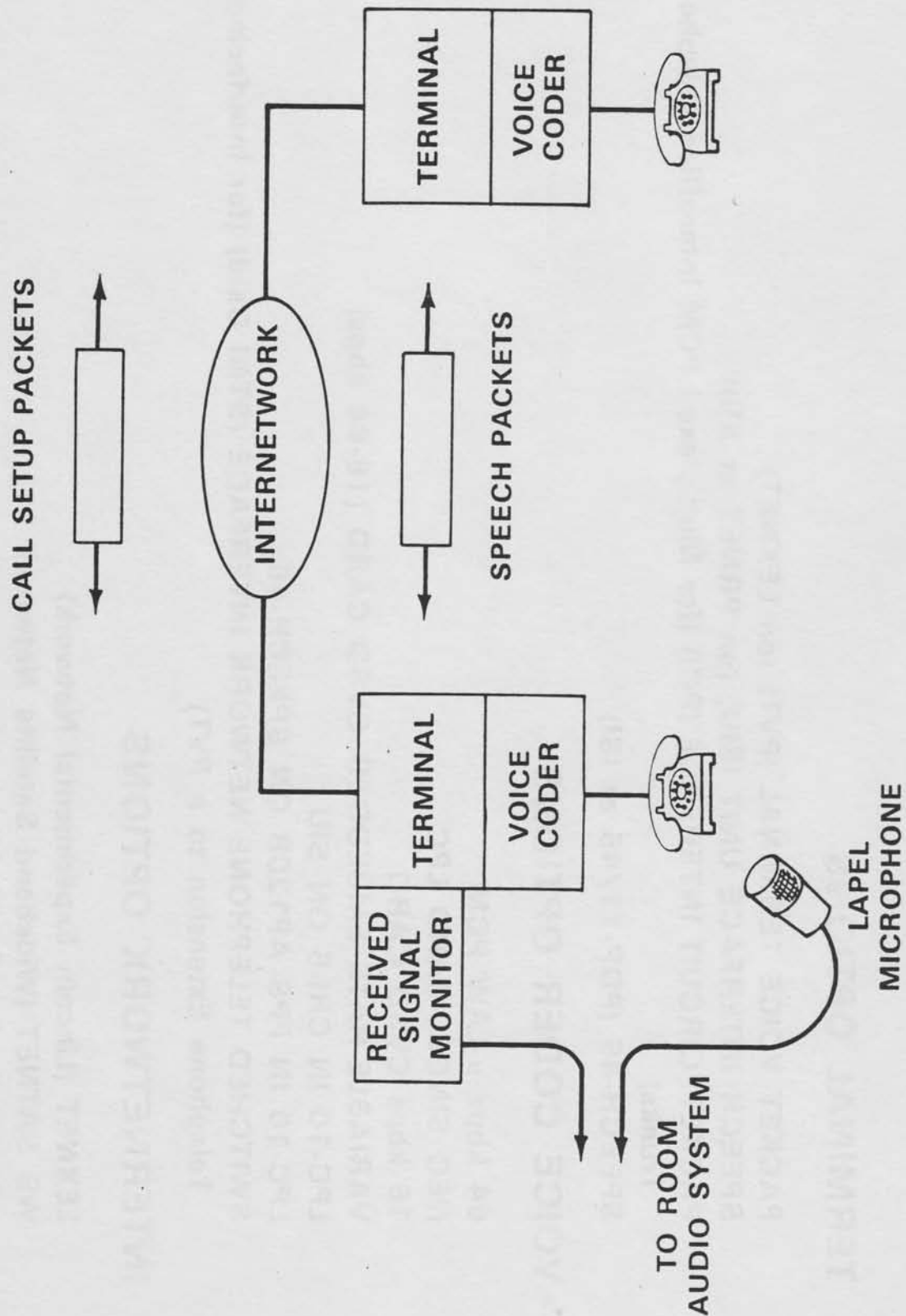
CONFERENCE

7. 3-SITE, 4-PARTY LPC CONFERENCE
LL (2 PARTIES ON LEXNET)
ISI (ON LEXNET)
SRI (ON PRNET UNIT IN SPEECH LAB, USING CHI-V LPC
AND SIU)

POINT-TO-POINT (MOBILE)

8. LPC SRI (MOBILE PRNET UNIT) - LL (LEXNET PVT)
MOBILE VAN RUN DEMONSTRATING PRNET SPEECH AND
ALTERNATE ROUTING

GENERIC PACKET VOICE CALL DEMO SETUP



TERMINAL OPTIONS

PACKET VOICE TERMINAL (PVT) (on LEXNET)
SPEECH INTERFACE UNIT (SIU) (on PRNET at SRI)
PACKET/CIRCUIT INTERFACE (PCI) (for Multiplexed PCM Interoffice Telephone Trunks)
SPEECH-45 (PDP-11/45 at ISI)

VOICE CODER OPTIONS

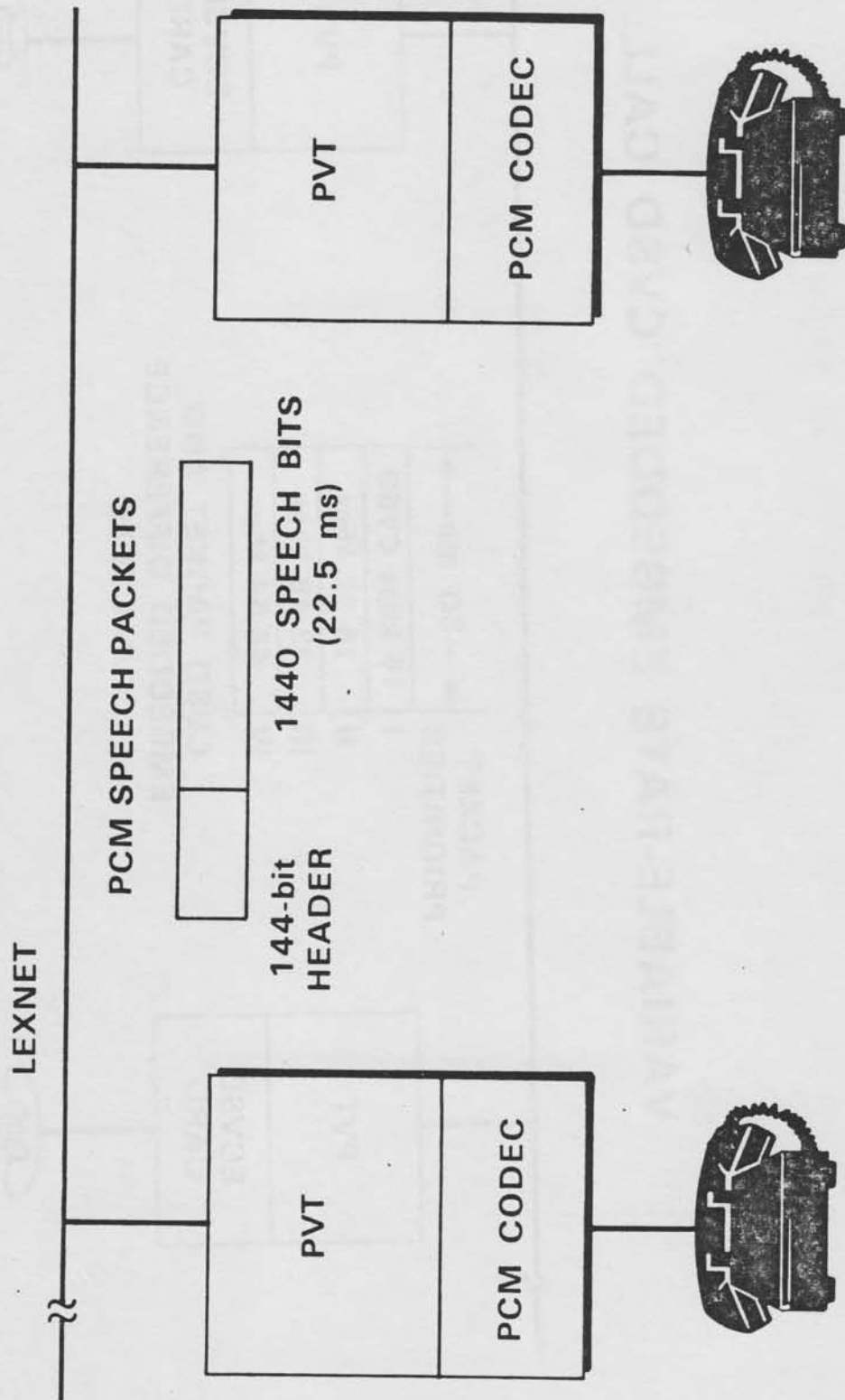
64 kbps μ -LAW PCM
NEC SINGLE-CARD LPC
16 kbps CVSD CARD
VARIABLE-RATE EMBEDDED CVSD CARD (16-64 kbps)
LPC-10 IN CHI-5 ON SIU
LPC-10 IN FPS AP120B ON SPEECH-45
SWITCHED TELEPHONE NETWORK INTERFACE (STNI Card) (for Interfacing a Telephone Extension to a PVT)

INTERNETWORK OPTIONS

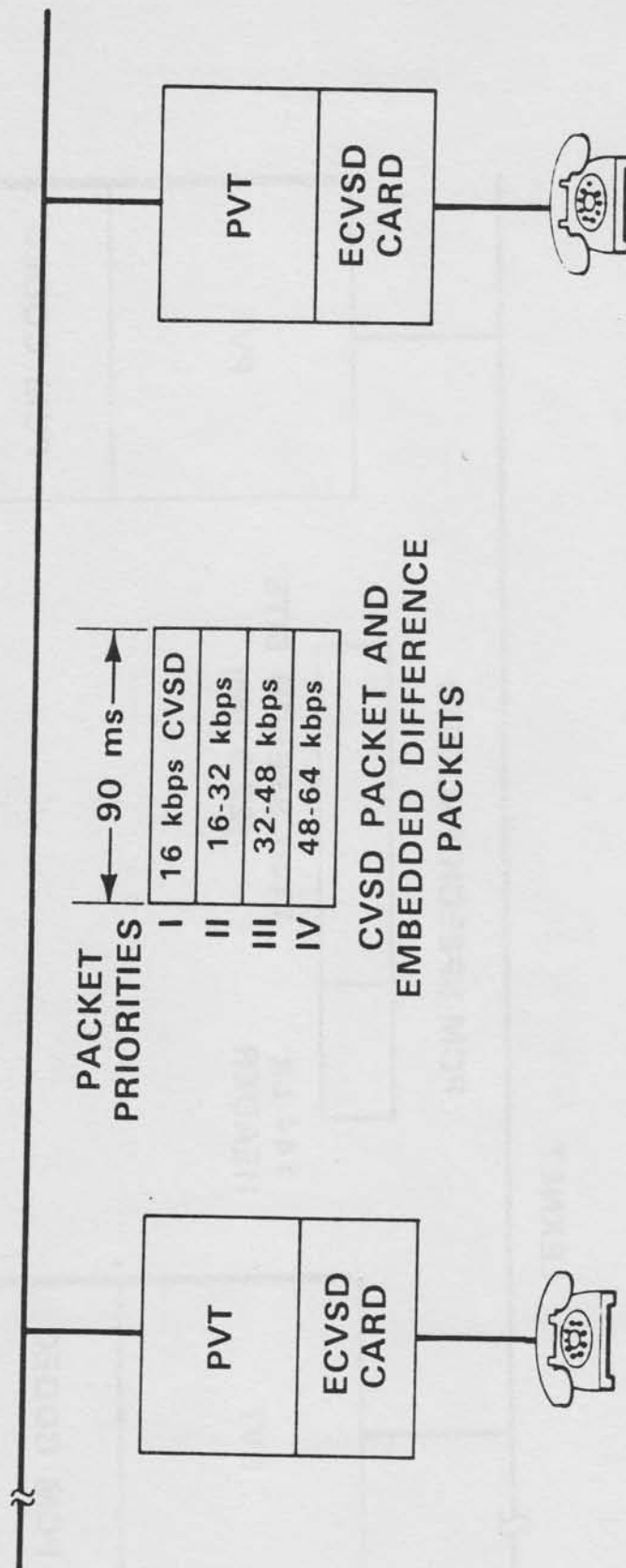
LEXNET (Lincoln Experimental Network)
WB SATNET (Wideband Satellite Network)
PRNET (Packet Radio Network)
Switched Telephone Net



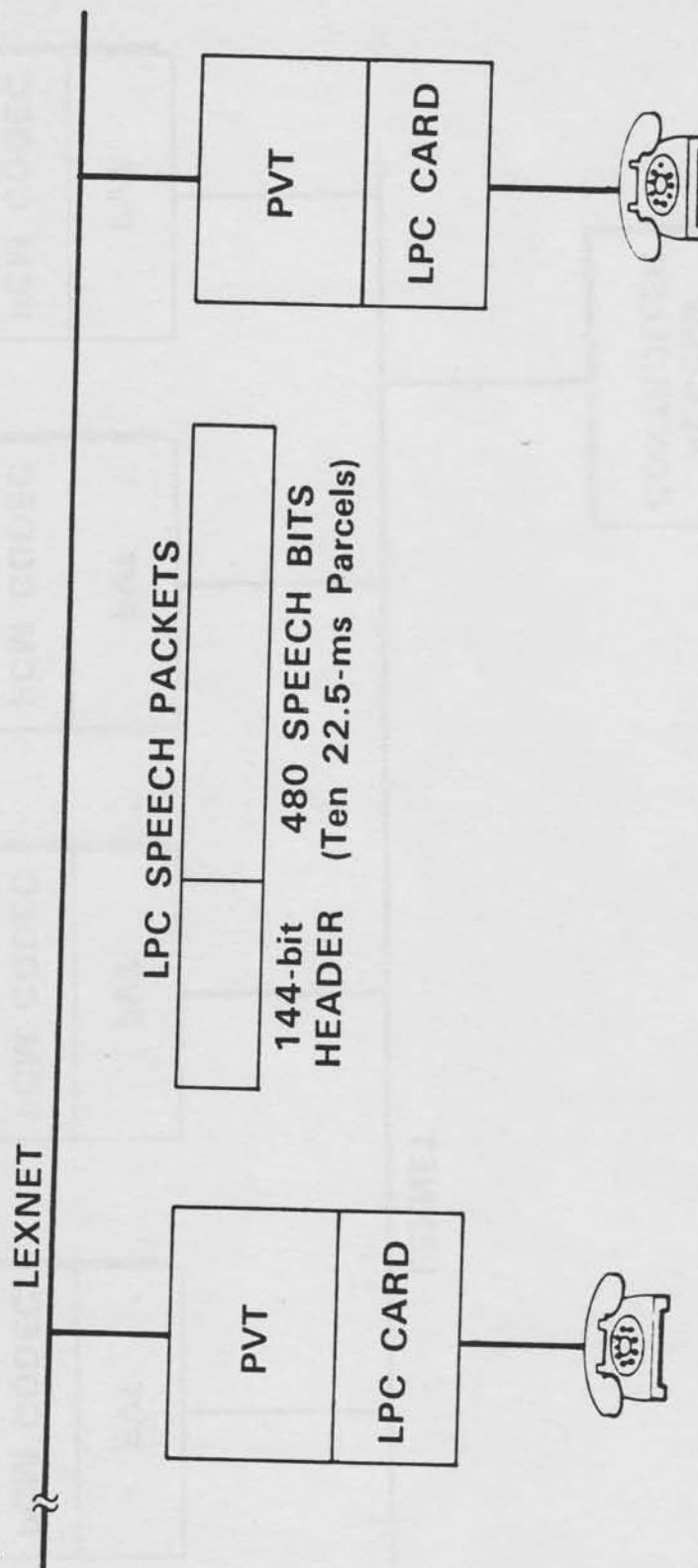
LOCAL POINT-TO-POINT 64 kbps PCM CALL



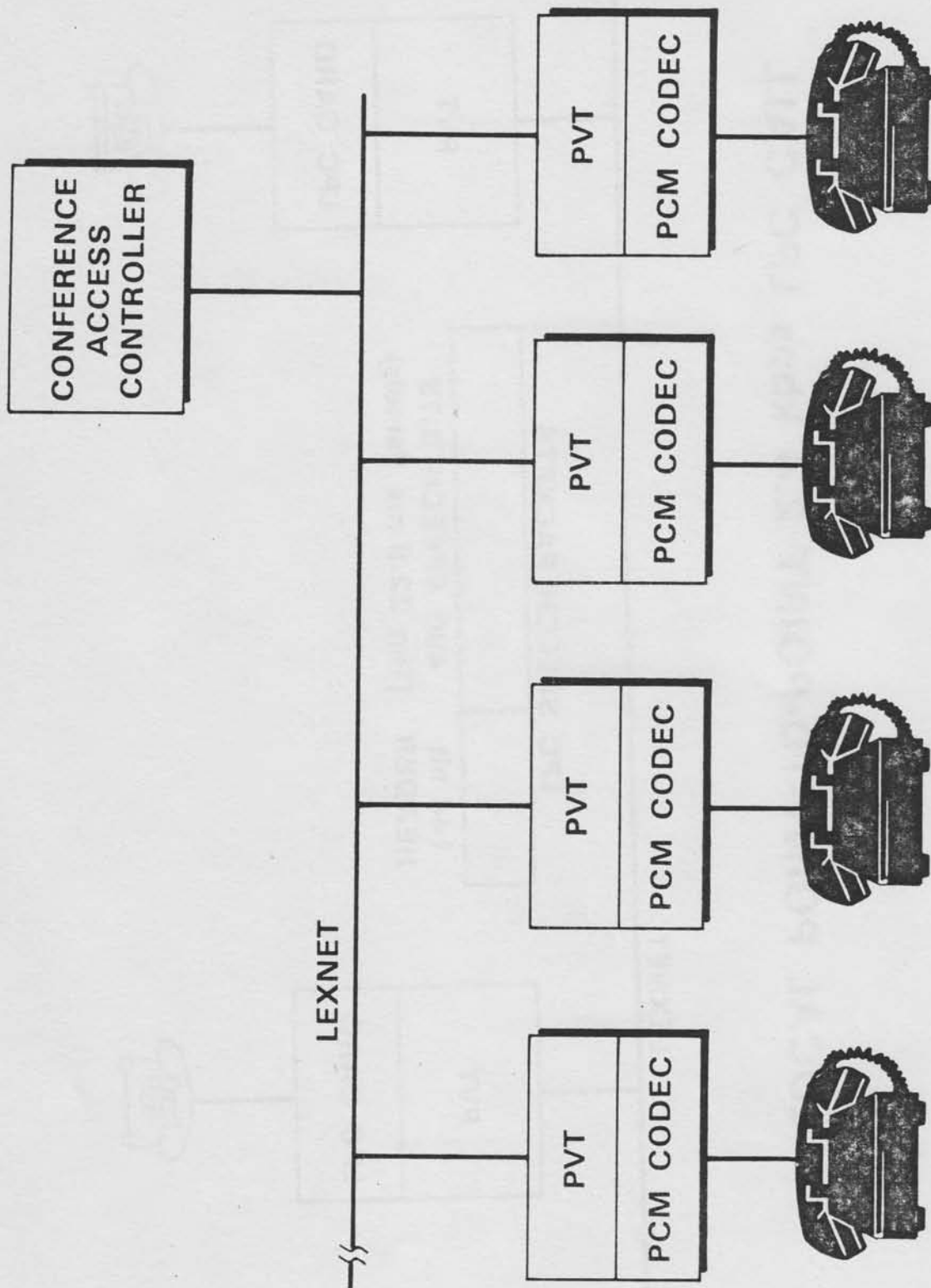
VARIABLE-RATE EMBEDDED CVSD CALL



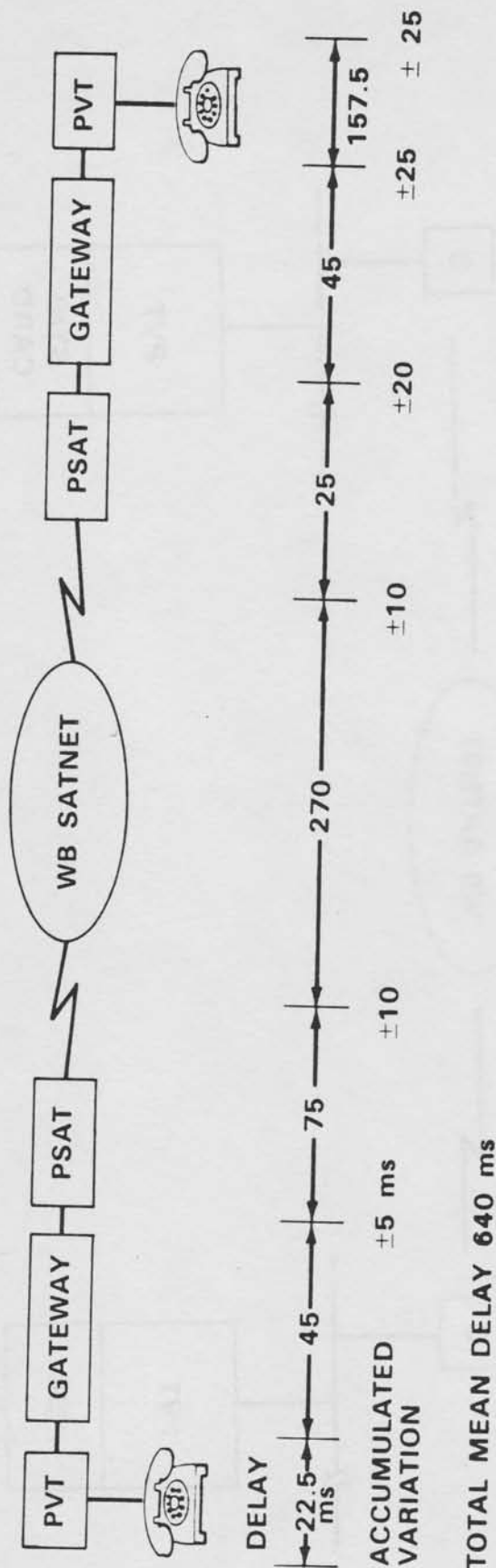
LOCAL POINT-TO-POINT 2.4 kbps LPC CALL



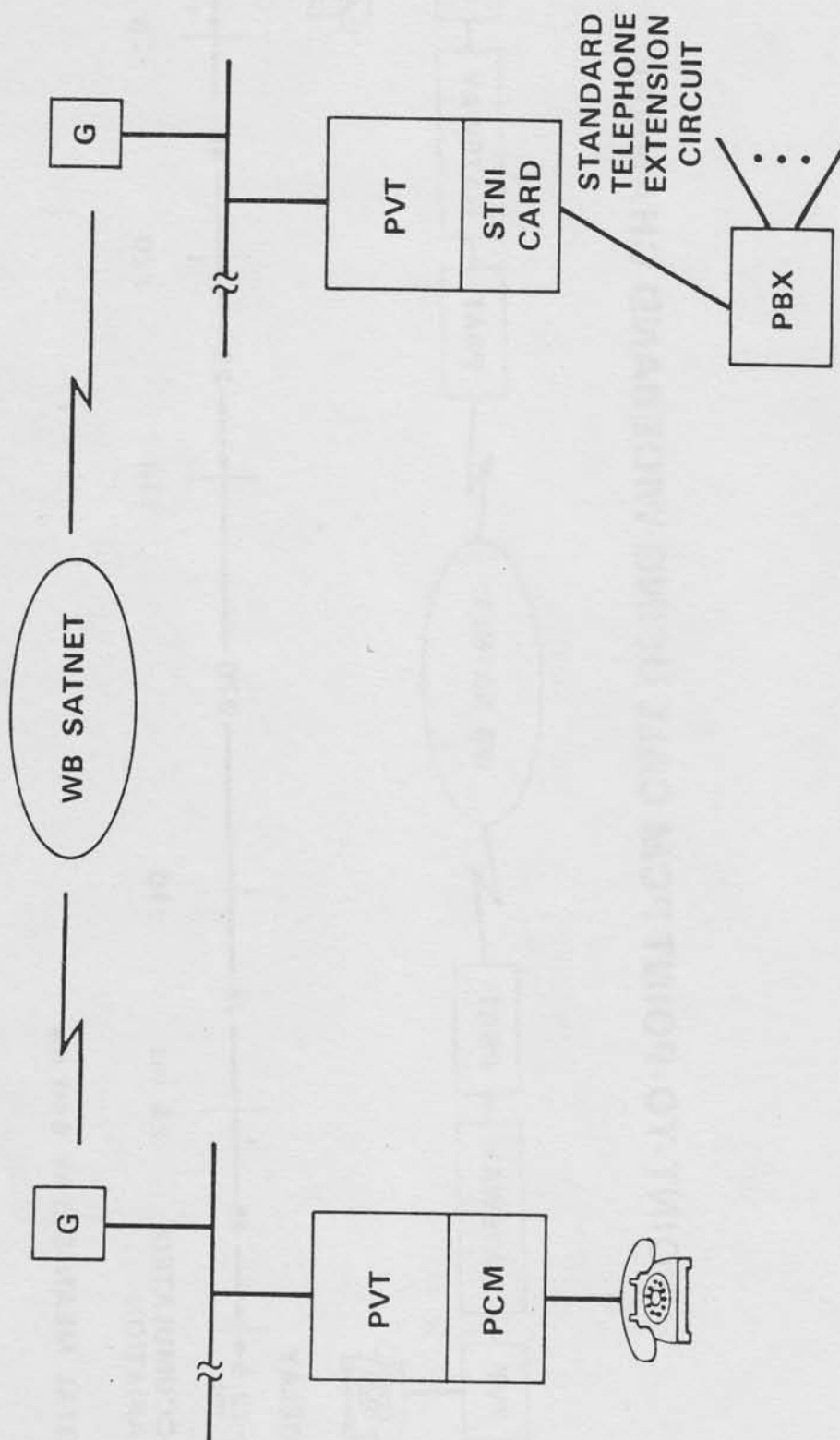
LOCAL PCM CONFERENCE



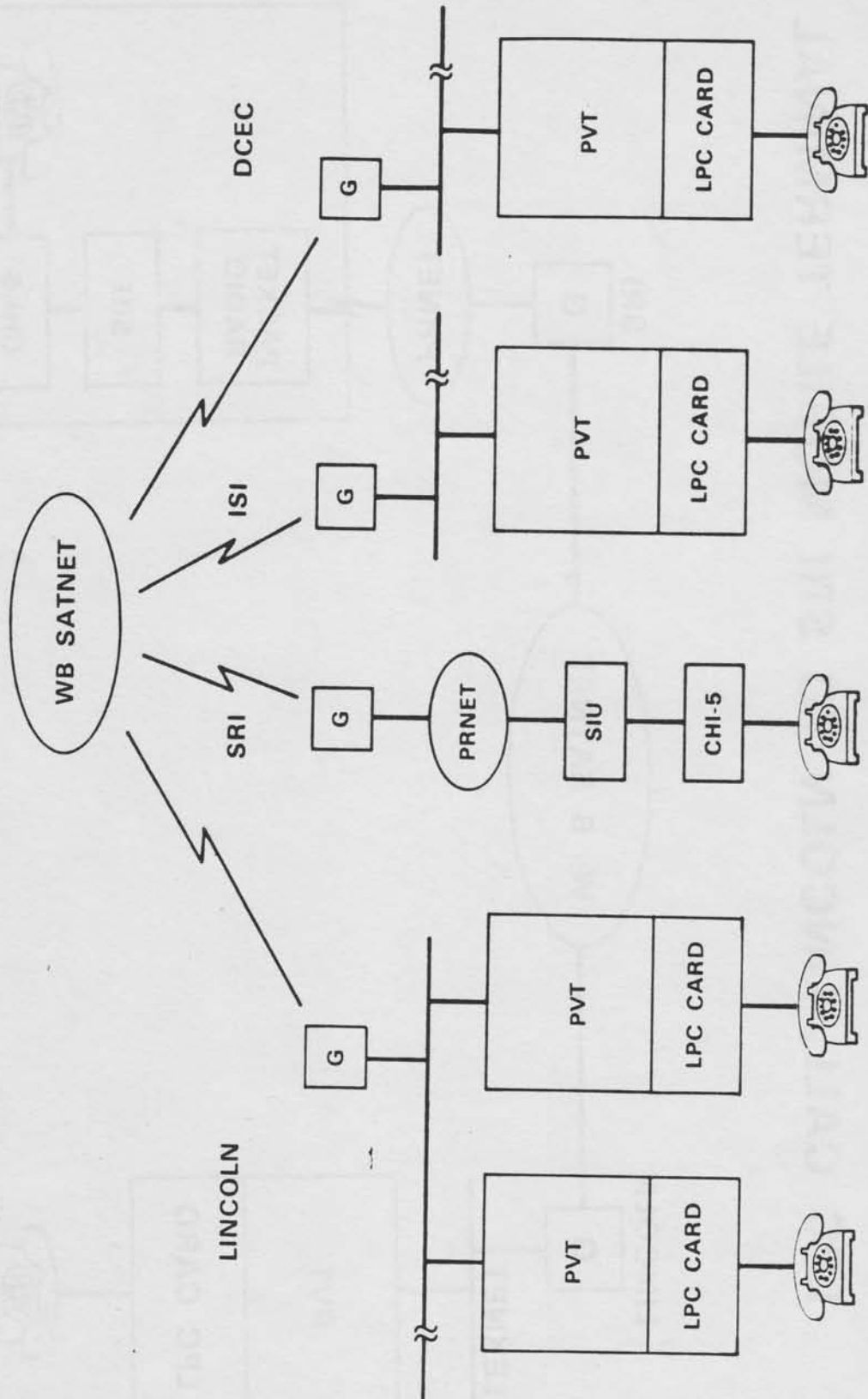
POINT-TO-POINT PCM CALL USING WIDEBAND CHANNEL



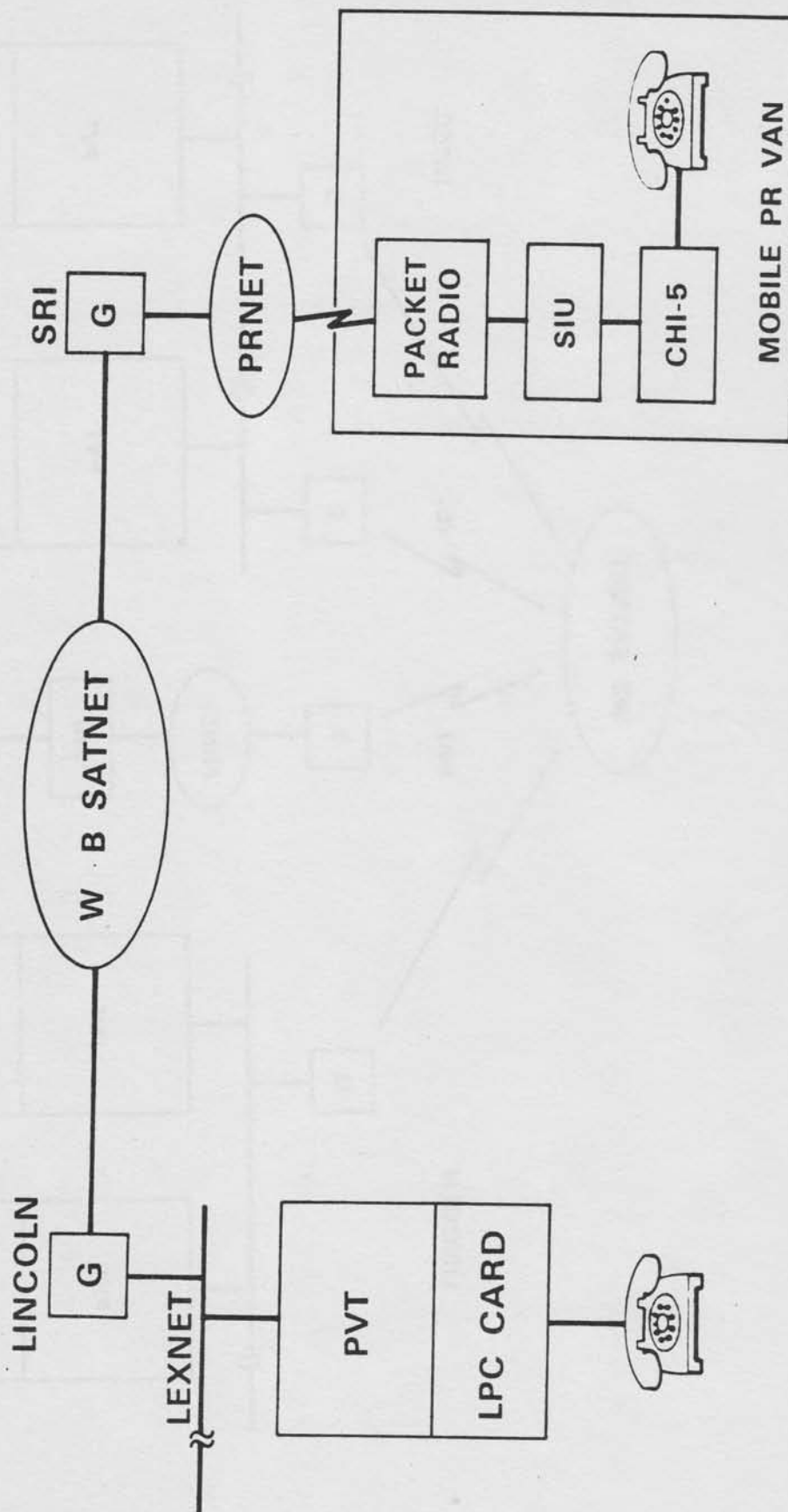
PCM CALL TO REMOTE TELEPHONE EXTENSION

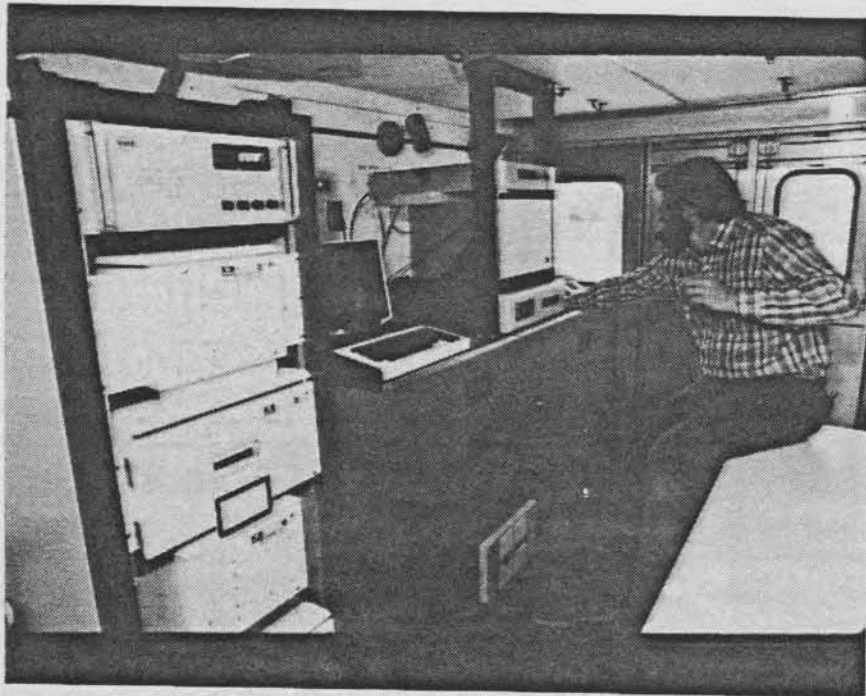


LPC CONFERENCE CALL



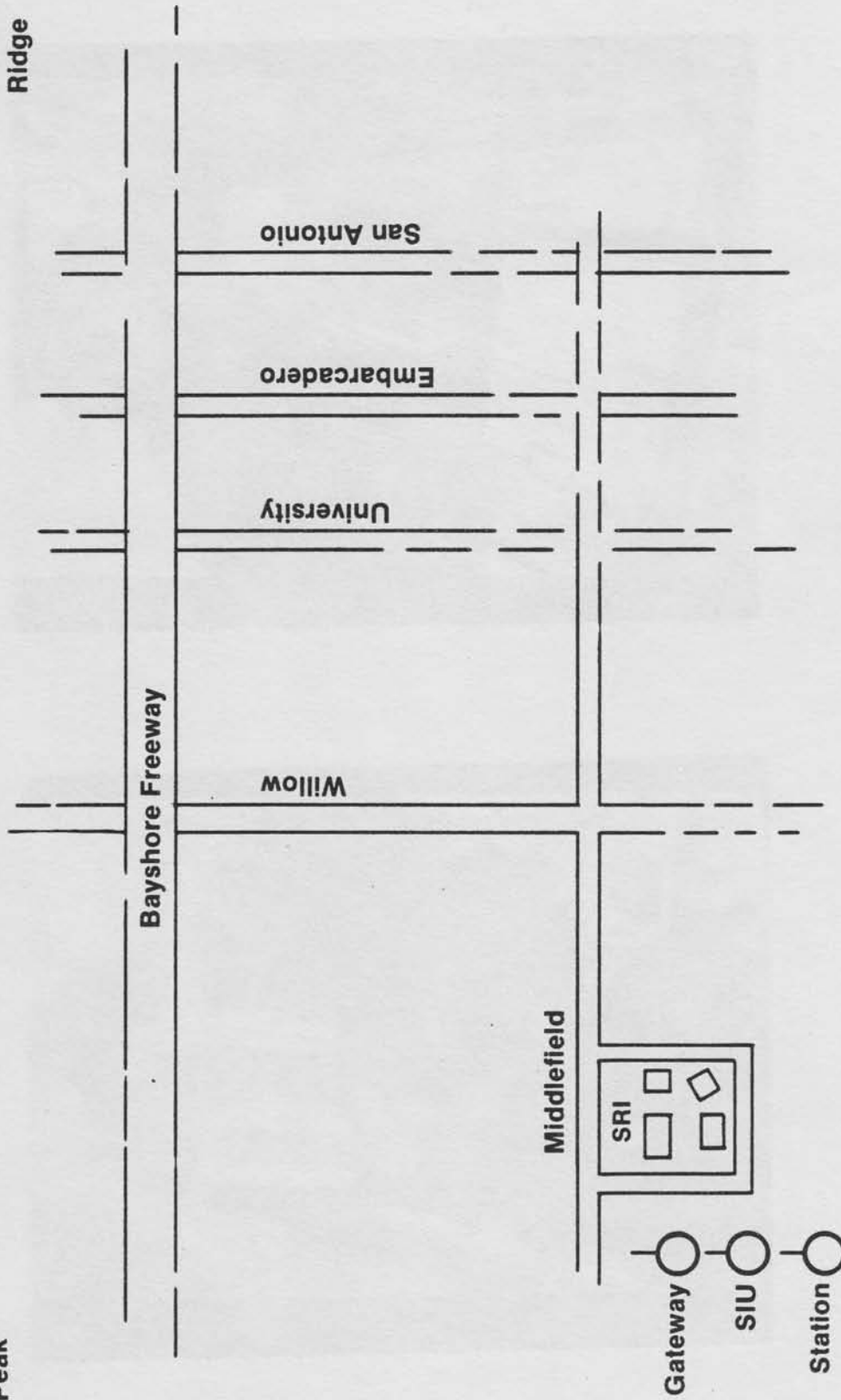
LPC CALL, LINCOLN TO SRI MOBILE TERMINAL





Grizzly
Peak

Mission
Ridge



Mission Ridge

San Antonio

Embarcadero

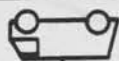
University

Willow

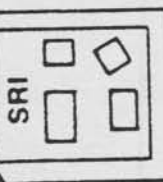
Bayshore Freeway

Eichler

Grizzly Peak



Middlefield

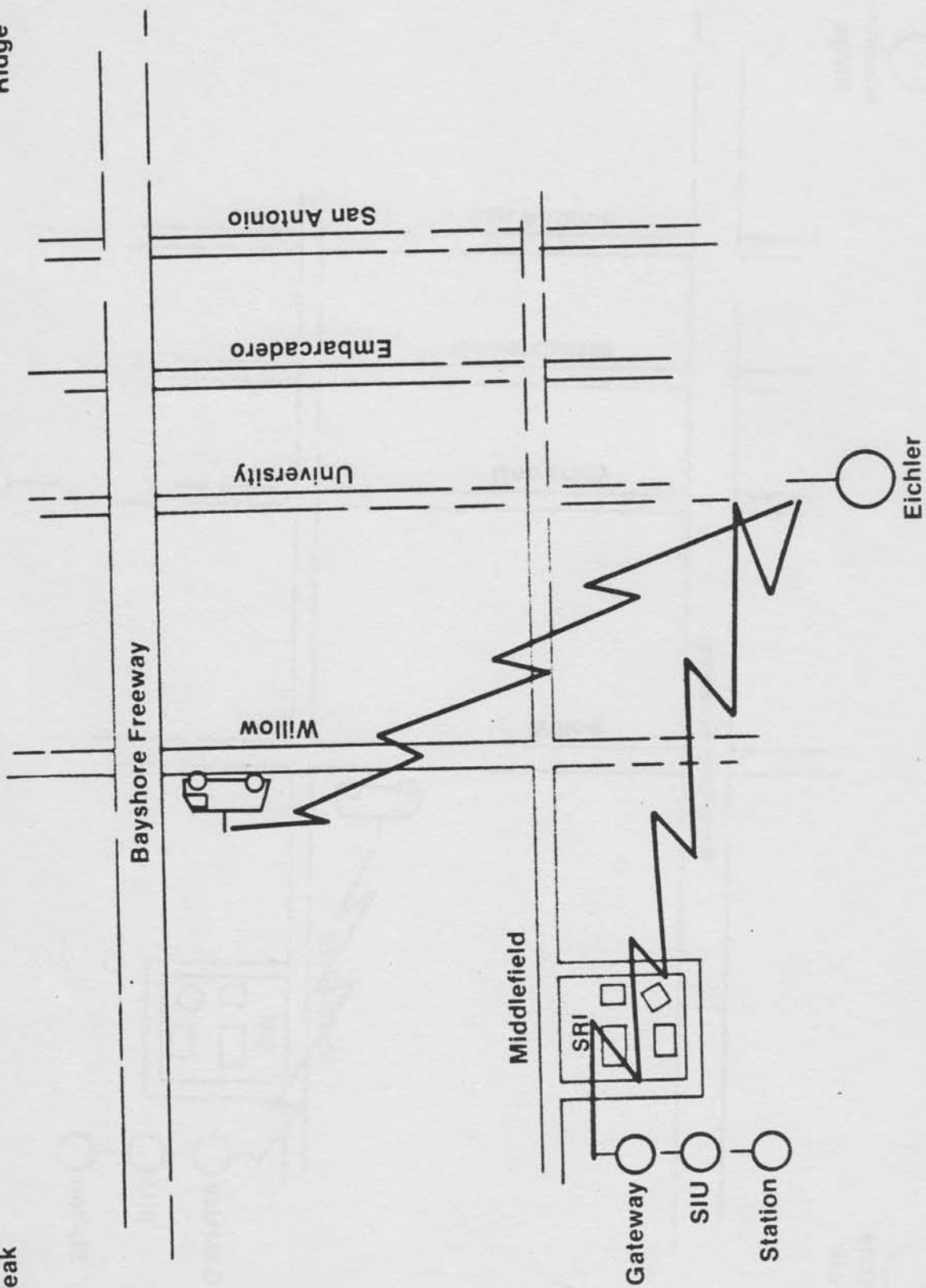


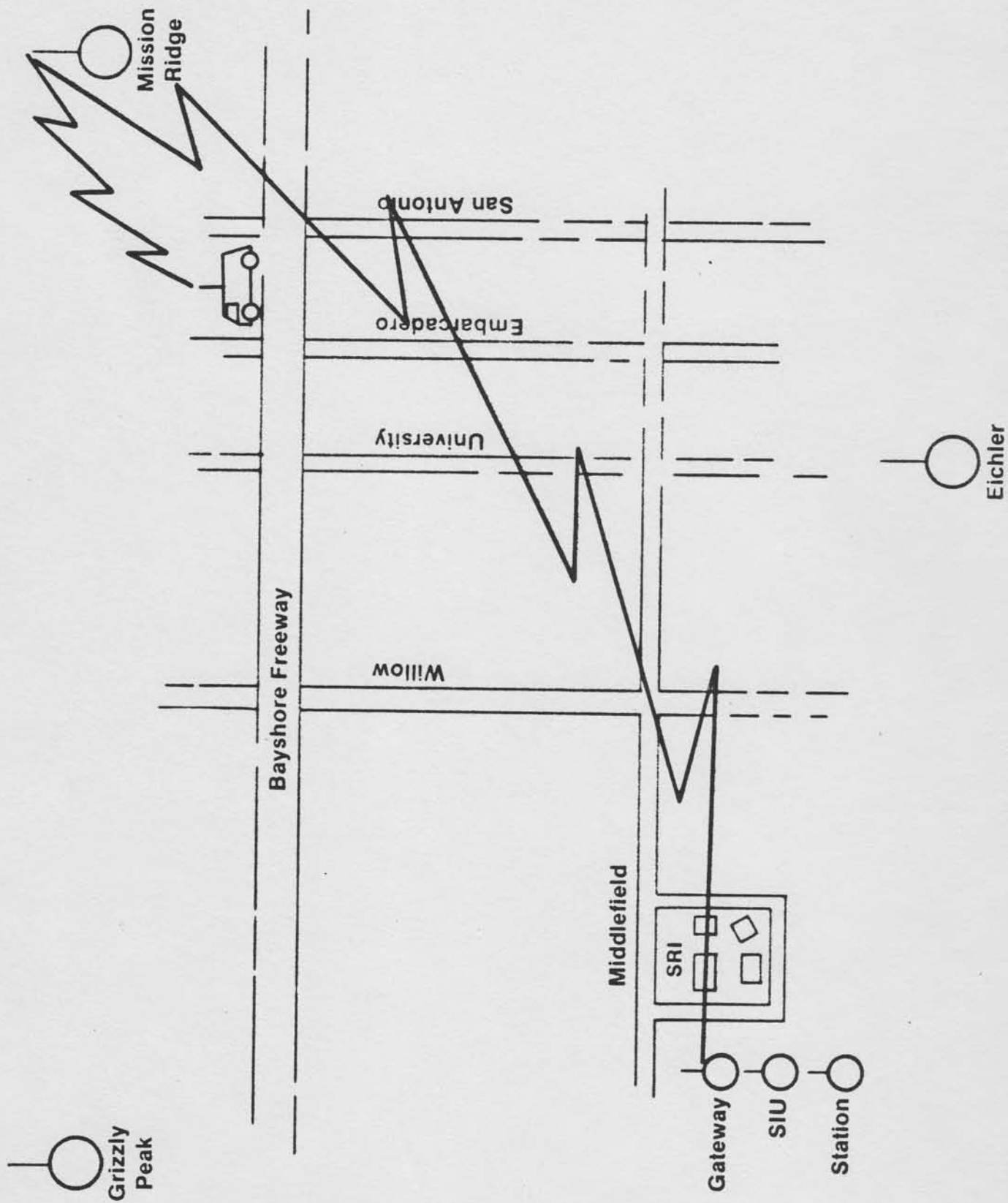
Gateway

SIU

Station

Mission Ridge





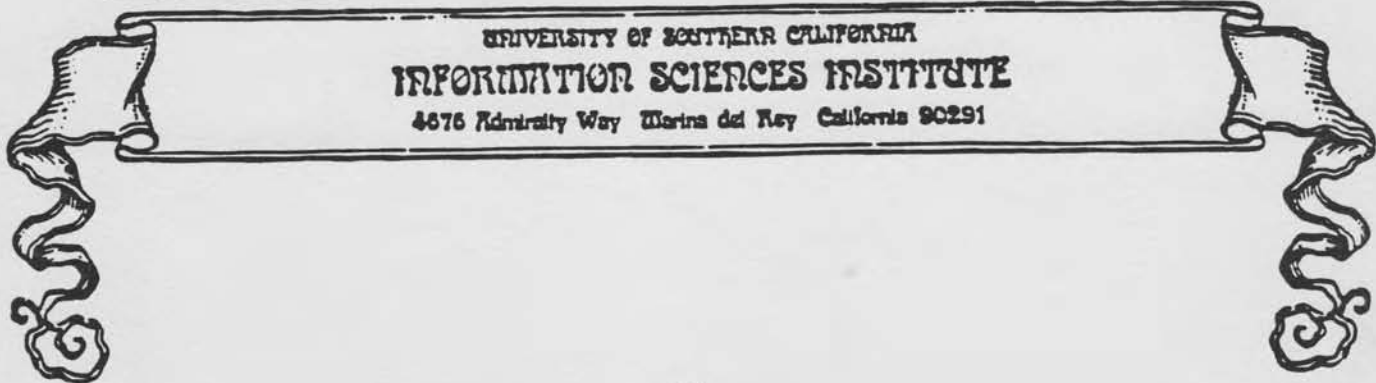


JSI

**NETWORK
VOICE
PROTOCOLS**



Danny Cohen



UNIVERSITY OF SOUTHERN CALIFORNIA
INFORMATION SCIENCES INSTITUTE
4676 Admiralty Way Marina del Rey California 90291

The History of Network Voice Protocols

In the beginning ARPA created the ARPAnet. Now the Network was formless and empty, Darkness was over the surface of the Deep....

And LGR said "Let there be protocols!" and there was NCP.

ARPA saw that the NCP was good and said "Use it for Packet Voice!..."

Well,..... NCP was not exactly the right Host/Host protocol for online speech.

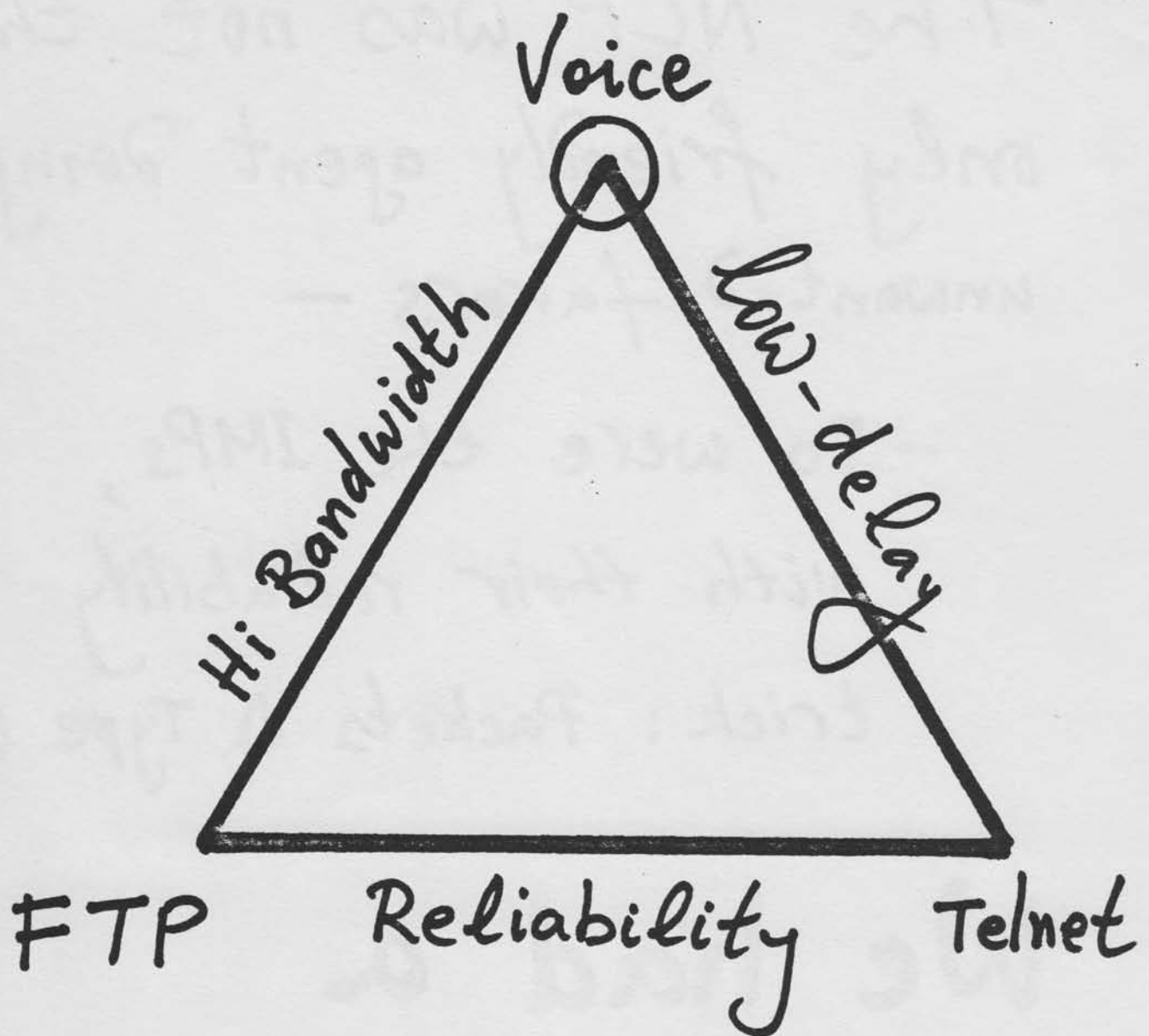
The NCP provided more favors than online-voice needed, at a non-trivial expense.

Therefore the need for NVP was recognized.

The NCP was not the only friendly agent doing unwanted favors -

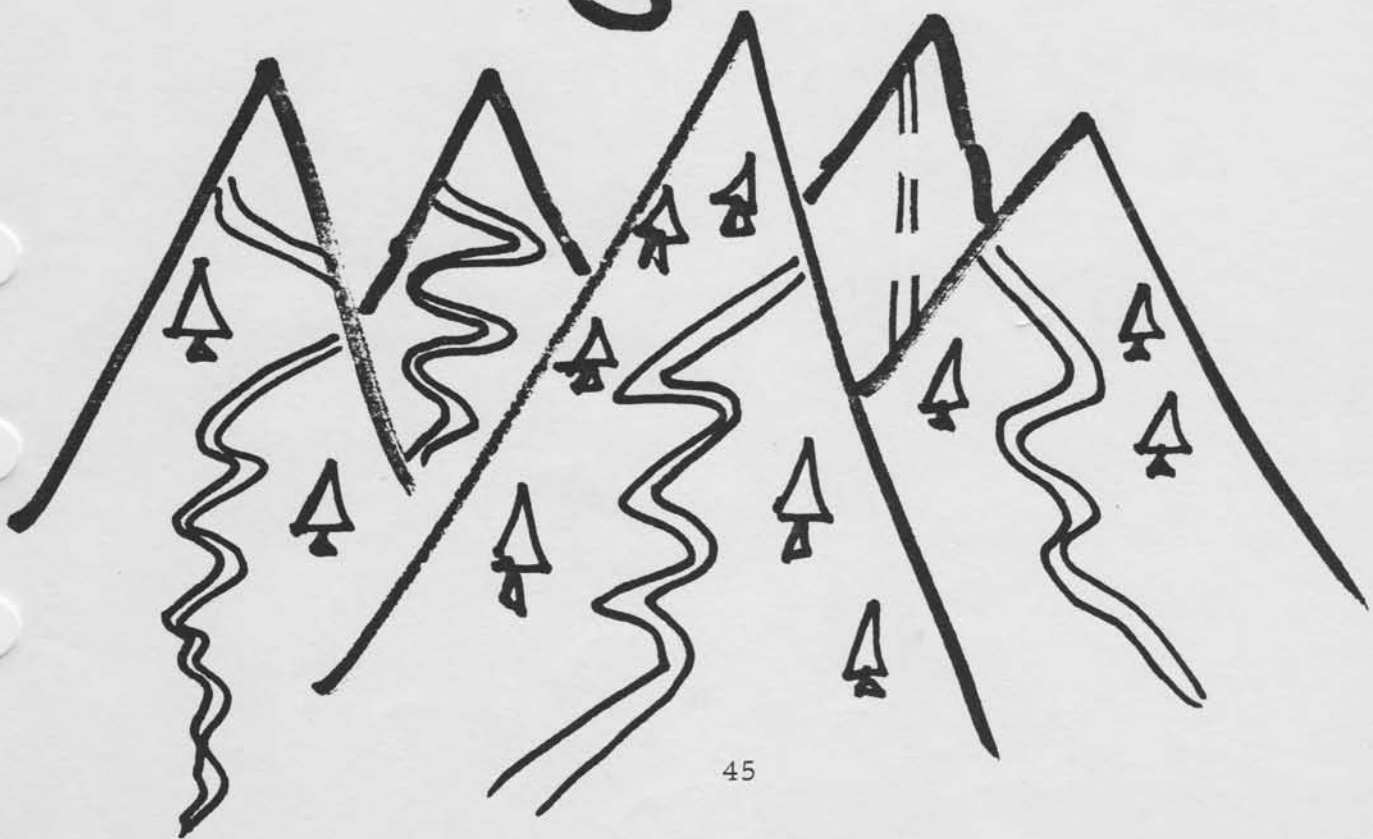
- So were the IMPs,
with their reliability
trick: Packets of Type 0

We had a
problem...



The Arpanet protocols were not designed for real-time applications

So we had to
think about it
until the next
meeting....



Objectives for NVP

- * Real time Data
- * Extensible (vocoder indep)
- * Network independent
- * Separation of Data/Control

NVP-0 was the
the first voice
protocol, a
precursor to NVP-1.

It was used for
some CVSD
experiments.

NVP-I was used
for most of the
experiments:

CVSD, LPC-I, LPC-II

NVP-I was
extended to
support Conferencing

NVCP

and voice-mail

When the PRNet
was born we were
expected to run
online realtime voice
to it by using

TCP

The thought of
using TCP for this
purpose was so
underwhelming
that the original
TCP became
IP + TCP

NVP-I was
modified to run on
top of IP, and
was also improved
in some areas.

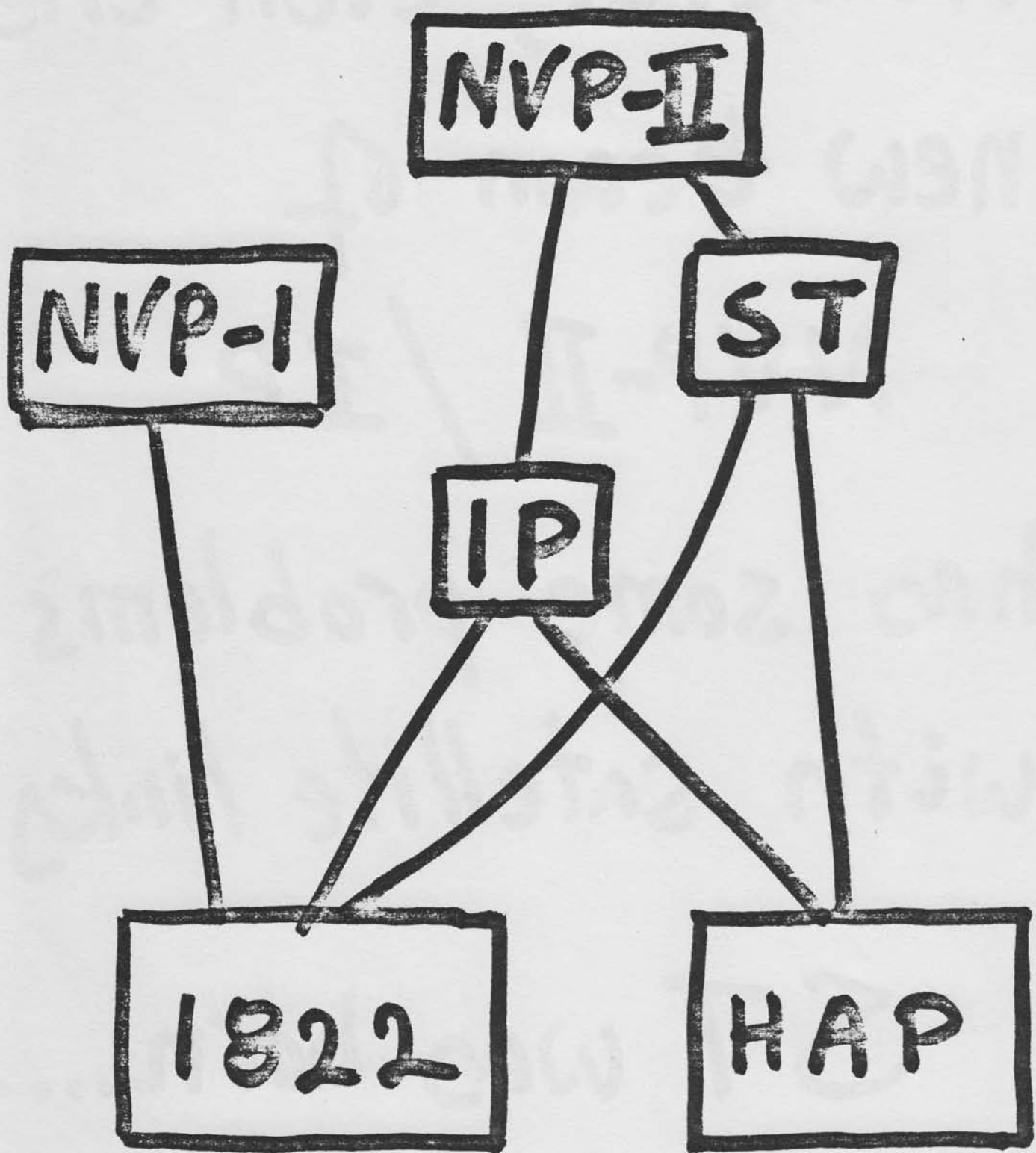
It became NVP-II

However, even the
new team of

NVP-II / IP

has some problems
with satellite links.

ST was born....



LESSONS

packet
communication
is practical for
online speech

Real-time data
needs a different
kind of protocol
than the standard
computer
communication

(reliability, flow control....)

Motivated
people and small
committees can
accomplish a lot.

Milestones in Packet Speech Communication

8/74: CVSD/ARPANet: $1S1+LL$

12/74: LPC/ARPANet: $LL+CH1$

1/76: LPC-CONFERENCE/ARPANet: $1S1+LL+CH1+SR1$

4/77: Flanagan (BTL) applies for a patent on
packet transmission of speech

7/78: USA patent 4,100,377 granted

SUMMARY

The interest of
the various phone
companies in packet
voice is a significant
testimonial to our

SUCCESS

SPEECH CONFERENCING

JAMES W. FORGIE
MIT LINCOLN LABORATORY

OUTLINE

1. VOICE CONFERENCING SYSTEM DESIGN ISSUES
2. HISTORY OF PACKET CONFERENCING
3. CURRENT WB NET CONFERENCING SYSTEM

VOICE CONFERENCING SYSTEM DESIGN CHOICES

1. SUMMATION OR SIGNAL SELECTION
2. VOICE OR PUSH-BUTTON CONTROL
3. CENTRALIZED OR DISTRIBUTED CONTROL

PACKET CONFERENCING DEMONSTRATIONS

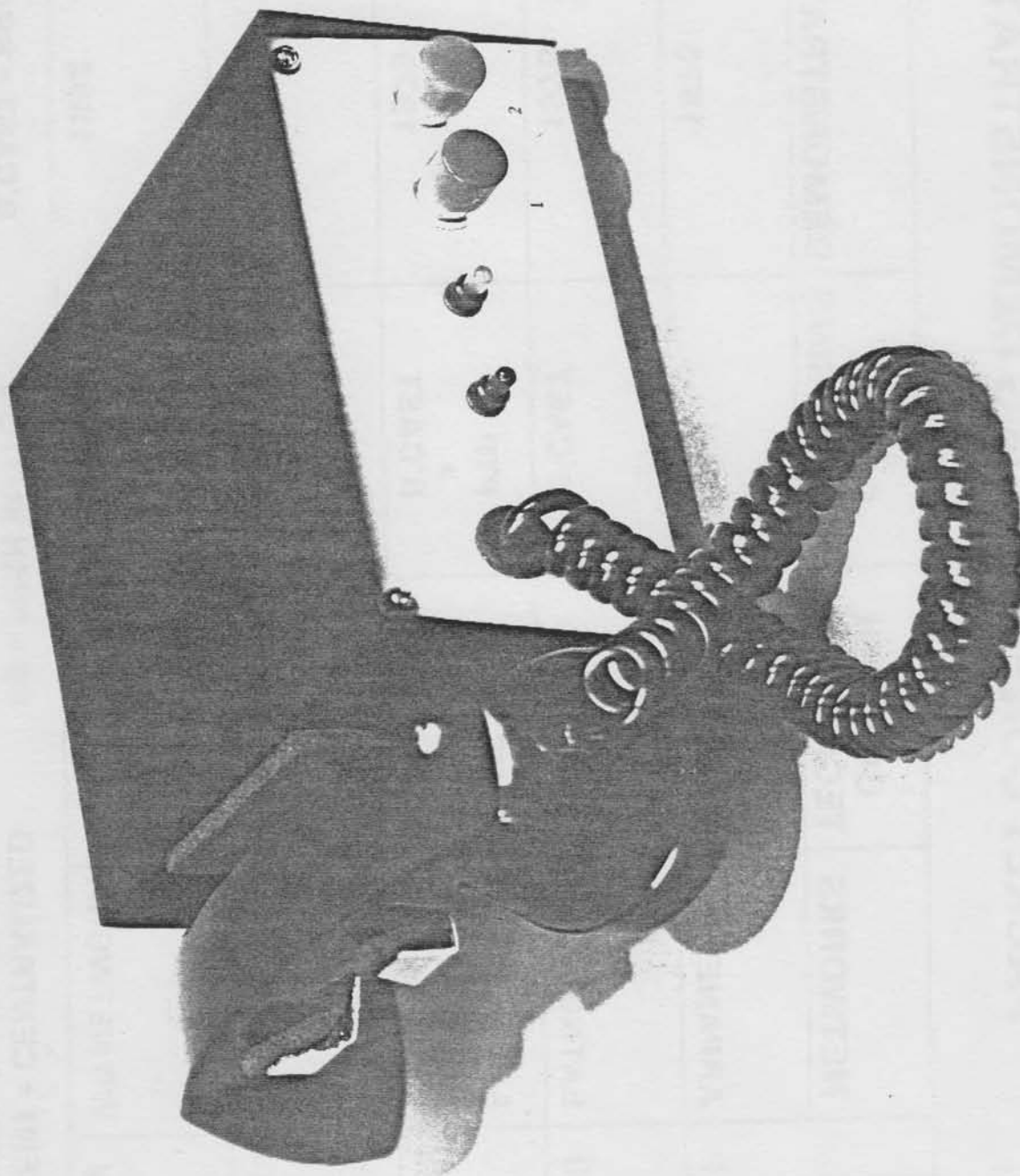
	NETWORKS	CONTROL TECHNIQUES		PACKET ADDRESSING	DEMONSTRATED	SITES
		CENT	PB			
I	ARPANET	CENT	PB	PTP	1976	CHI, ISI, SRI, LL
II	SATNET	DIST	PB	B'CAST	1978	NDRE, UCL, BBN
III	ARPANET + SATNET	CENT + DIST	PB	PTP + B'CAST	1979	ISI, LL + NDRE, UCL
IV	SATNET	DIST	VOICE	B'CAST	1979	NDRE, UCL, BBN
V	WB NETWORK	DIST	VOICE	B'CAST	1982	ISI, SRI, LL

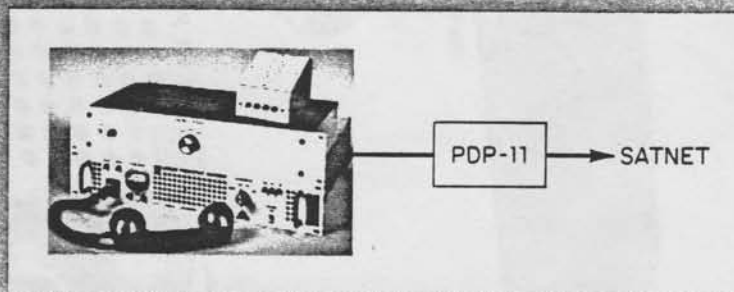
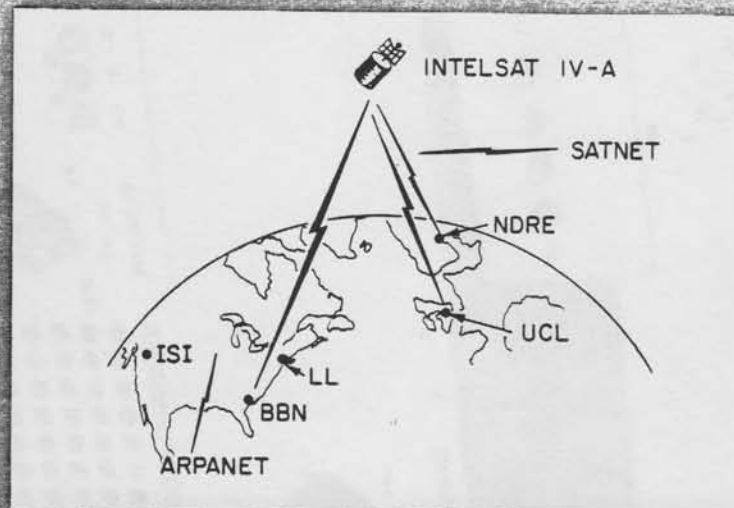
CENT = CENTRALIZED
DIST = DISTRIBUTED

PB = PUSH BUTTON
PTP = POINT-TO-POINT

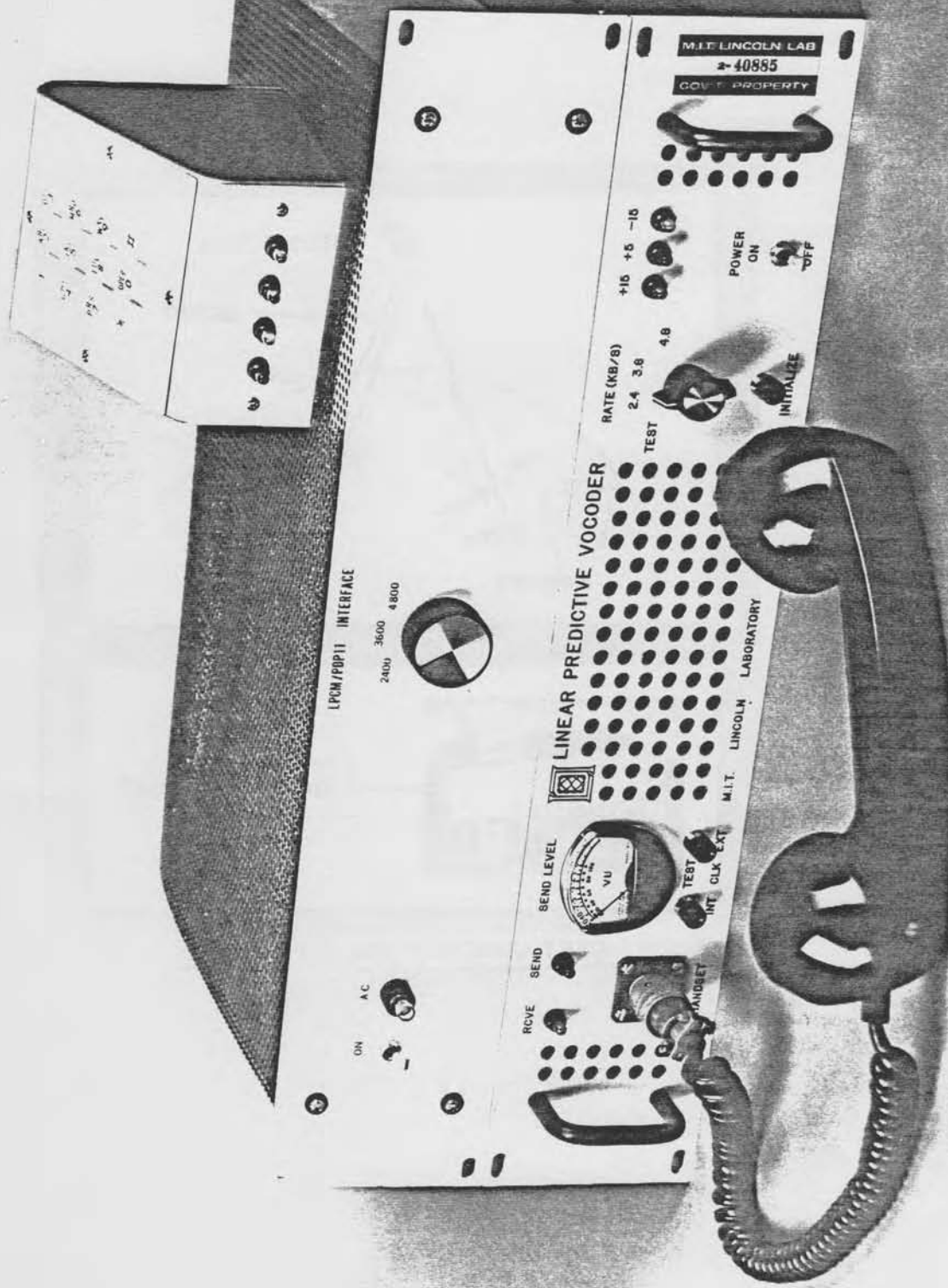
B'CAST = BROADCAST



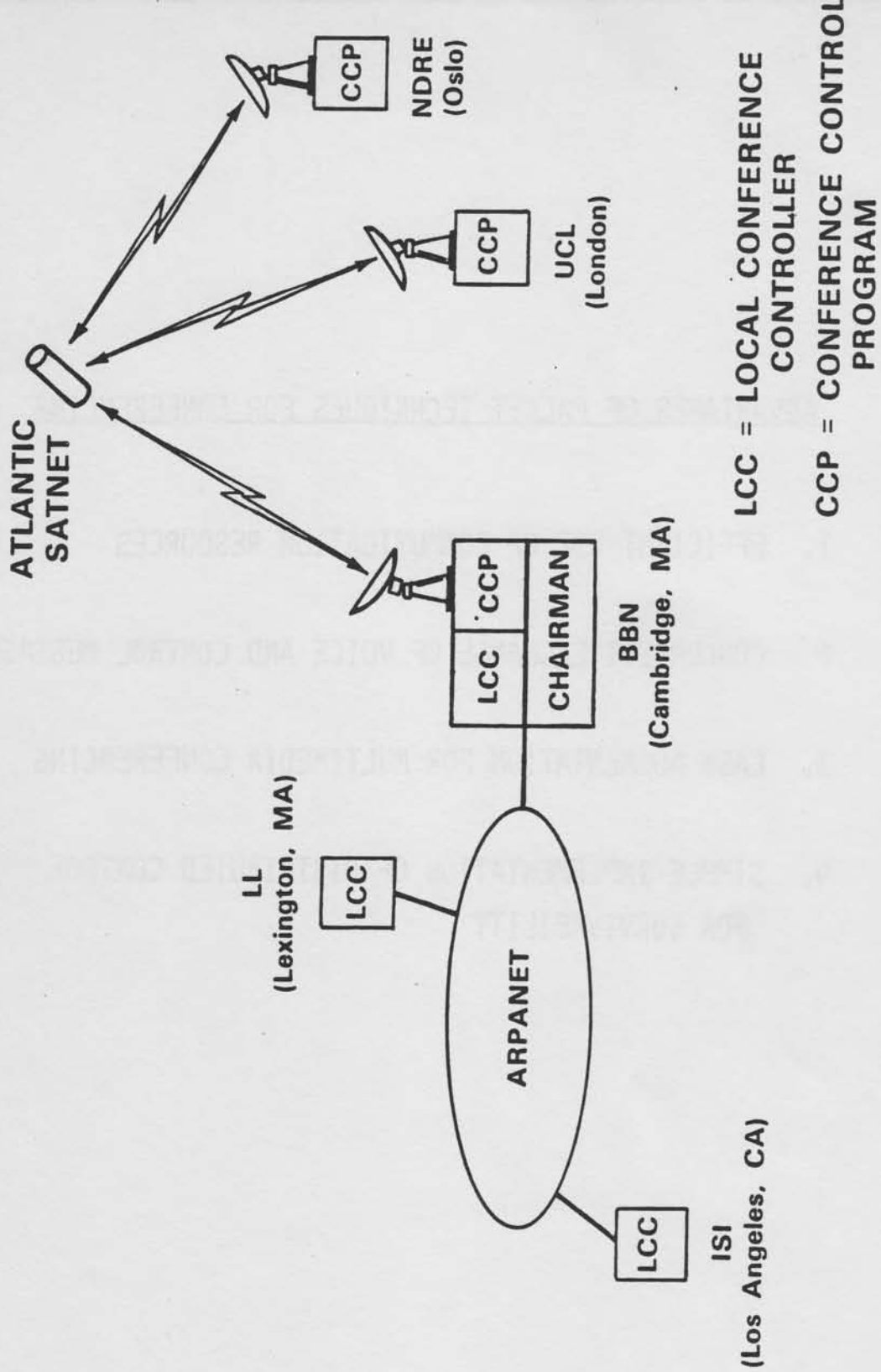




PACKET CONFERENCING EXPERIMENTS



SATNET/INTERNET VOICE CONFERENCING



ADVANTAGES OF PACKET TECHNIQUES FOR CONFERENCING

1. EFFICIENT USE OF COMMUNICATION RESOURCES
2. CONCURRENT EXCHANGE OF VOICE AND CONTROL MESSAGES
3. EASY AUGMENTATION FOR MULTIMEDIA CONFERENCING
4. SIMPLE IMPLEMENTATION OF DISTRIBUTED CONTROL
FOR SURVIVABILITY

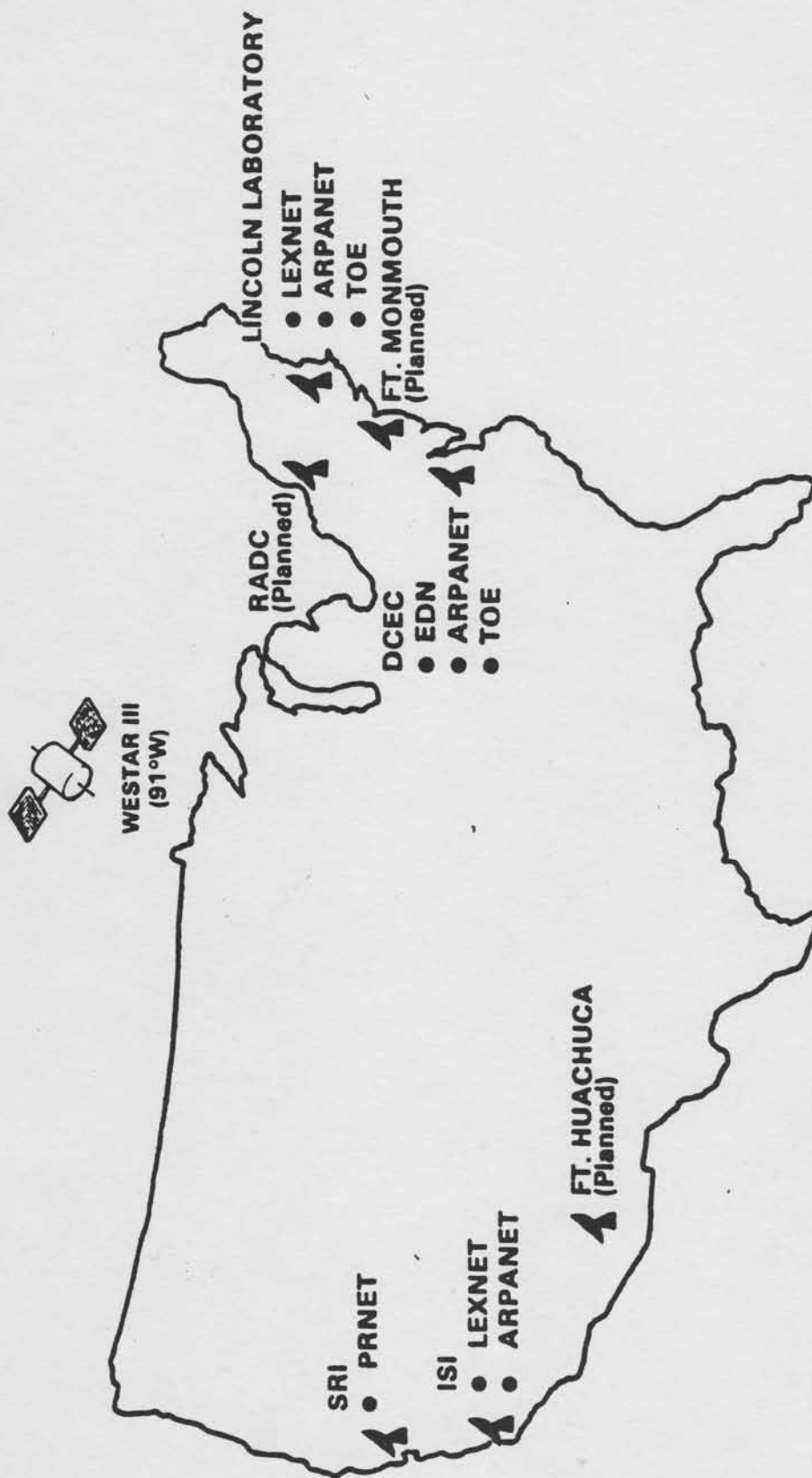
WIDEBAND INTEGRATED VOICE/DATA NETWORK

CLIFFORD J. WEINSTEIN
MIT LINCOLN LABORATORY

WIDEBAND INTEGRATED VOICE/DATA NETWORK

- MOTIVATION FOR WIDEBAND EXPERIMENT
- EXPERIMENTAL SYSTEM DESCRIPTION
- CHANNEL ASSIGNMENT AND PACKET MULTIPLEXING
- EXPERIMENT STATUS

WB SATNET TOPOLOGY



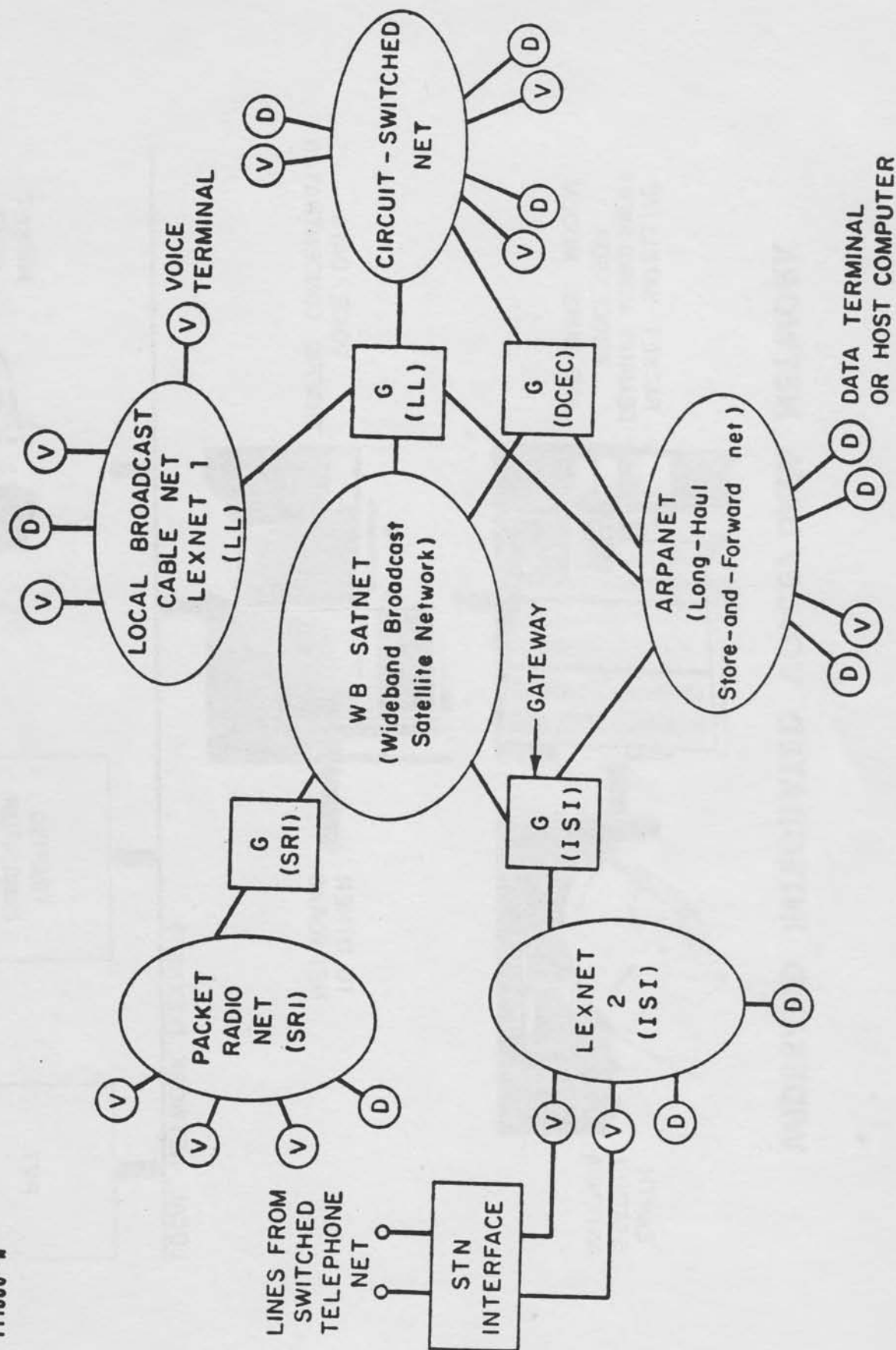
LEXNET = LOCAL PACKET VOICE NETWORK
 PRNET = PACKET RADIO NET
 TOE = TELEPHONE OFFICE EMULATOR

114814-N-01

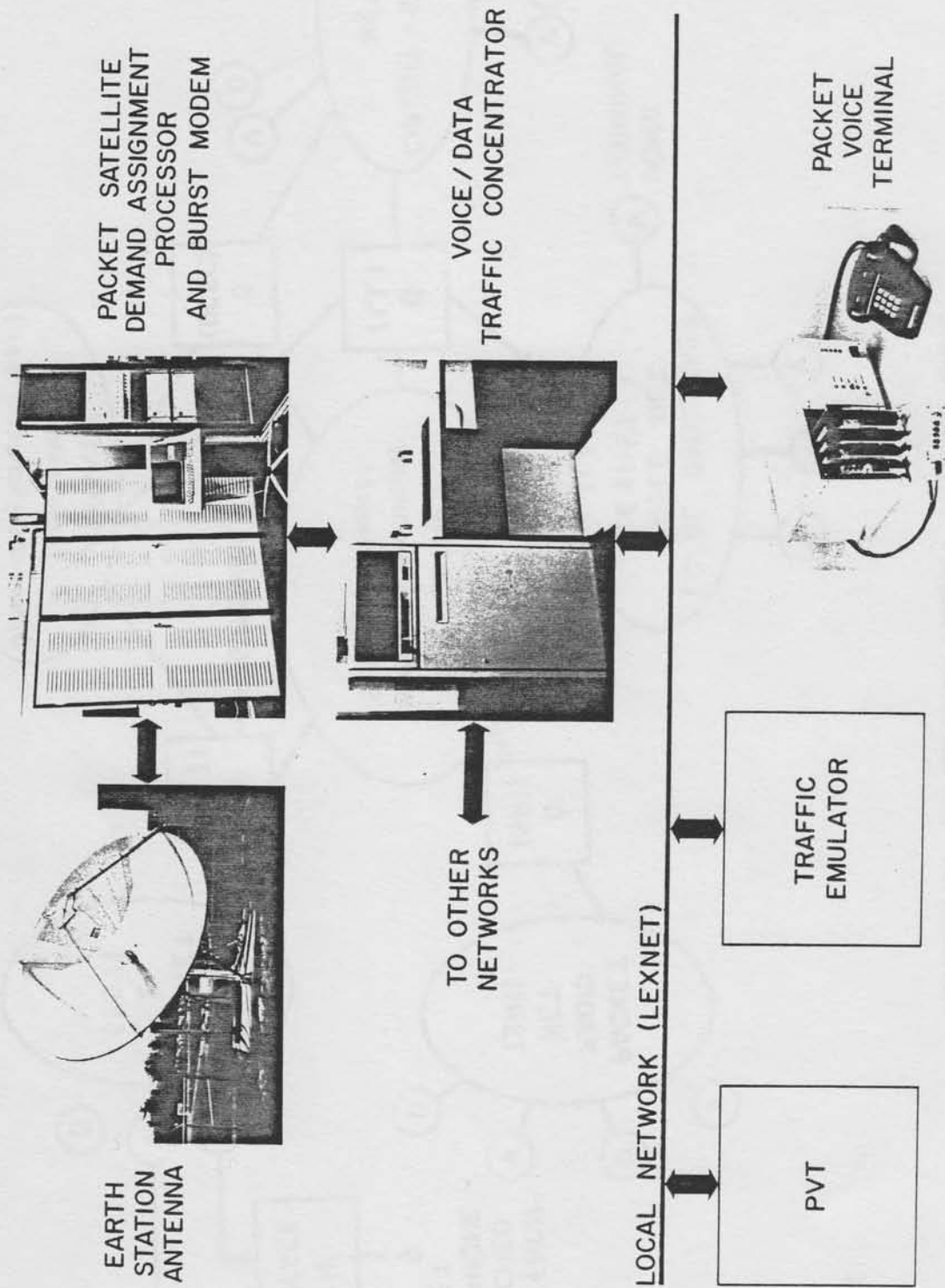


INTEGRATED VOICE/DATA PACKET INTERNETWORK

111686-N

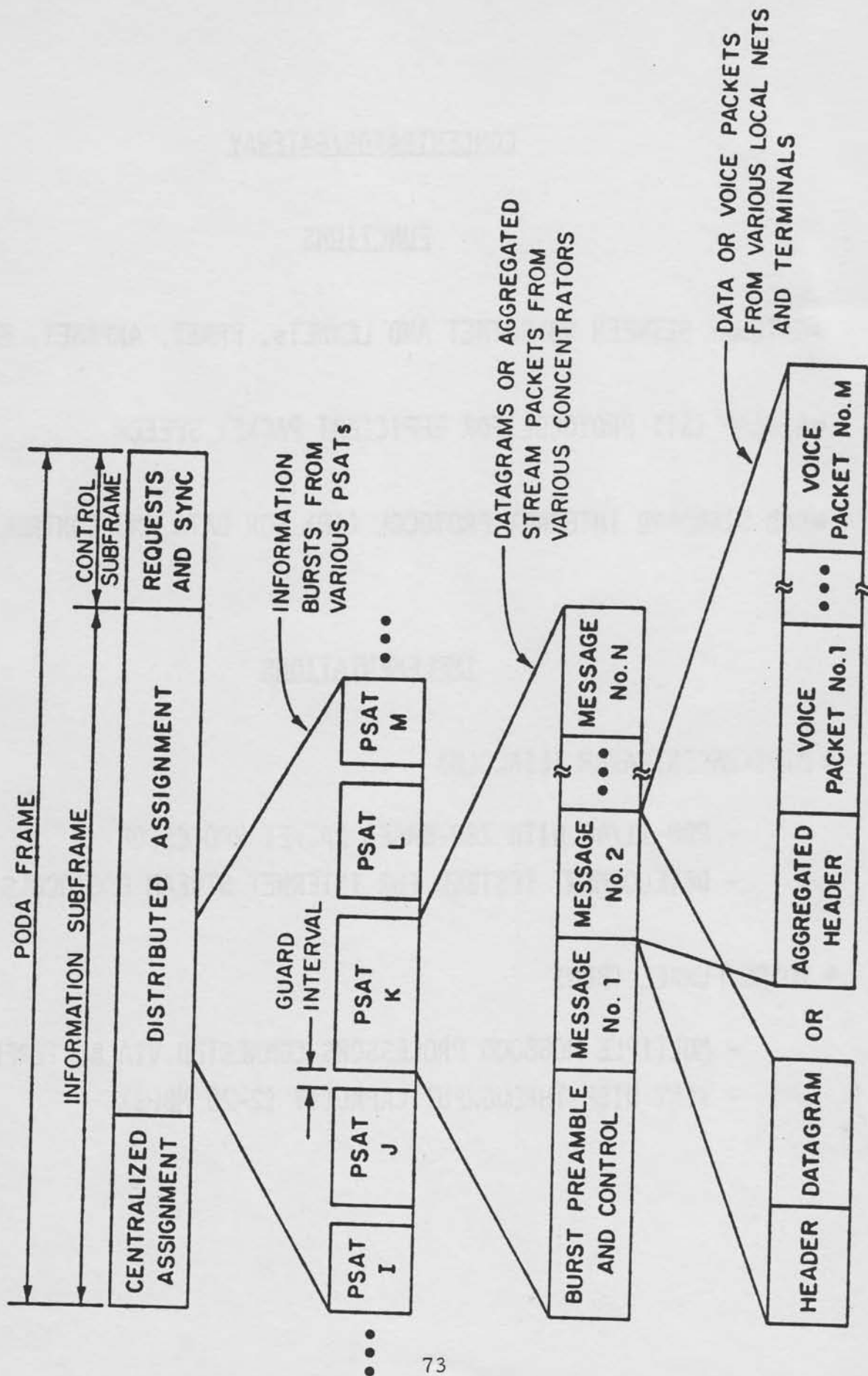


WIDEBAND INTEGRATED VOICE / DATA NETWORK



PACKET MULTIPLEXING HIERARCHY

111693-N



CONCENTRATOR/GATEWAY

FUNCTIONS

- GATEWAY BETWEEN WB SATNET AND LEXNETs, PRNET, ARPANET, EDN
- STREAM (ST) PROTOCOL FOR EFFICIENT PACKET SPEECH
- DoD STANDARD INTERNET PROTOCOL (IP) FOR DATA AND CONTROL

IMPLEMENTATIONS

- MINICONCENTRATOR (LINCOLN)
 - PDP-11/44 WITH Z80-BASED PACKET PROCESSOR
 - DEVELOPMENT TESTBED FOR INTERNET STREAM PROTOCOLS
- VOICE FUNNEL (BBN)
 - MULTIPLE MC68000 PROCESSORS CONNECTED VIA BUTTERFLY SWITCH
 - VERY HIGH THROUGHPUT CAPACITY (2-20 MBPS)

WIDEBAND NETWORK SPEECH EXPERIMENT MILESTONES

18 NOV 81	LL TO ISI (PCM, 2 CONVERSATIONS, ONE USING STNI AT ISI)					
22 JAN 82	<table border="0"><tr><td>PCI → PCI</td><td rowspan="2">} VIA SATELLITE</td><td rowspan="2">{ 2 HOSTS ON LL PSAT</td></tr><tr><td>PCI → LEXNET</td><td>{ 2 CONVERSATIONS</td></tr></table>	PCI → PCI	} VIA SATELLITE	{ 2 HOSTS ON LL PSAT	PCI → LEXNET	{ 2 CONVERSATIONS
PCI → PCI	} VIA SATELLITE	{ 2 HOSTS ON LL PSAT				
PCI → LEXNET			{ 2 CONVERSATIONS			
3 FEB 82	FUNNEL AT LL TO GATEWAY AT ISI (PCM)					
22 FEB 82	PCI AT LL TO PCI AT DCEC (2 CONVERSATIONS)					
4 MAR 82	3-SITE SPEECH (LL, ISI, DCEC) IN 2-PARTY COMBINATIONS					
9 APR 82	FUNNEL AT LL TO FUNNEL AT ISI					
22 APR 82	SRI (LEXNET) TO ISI (LEXNET)					
7 MAY 82	SIMULTANEOUS LPC CALLS PVT (LL) → PRNET (CHI-V) AT SRI PVT (LL) → LEXNET (AP120B) AT ISI					
13 MAY 82	2-SITE (LL/ISI), 3-PARTY PCM CONF					
21 MAY 82	3-SITE LPC CONF: PVTs AT LL, ISI, SRI					
1 JUNE 82	3-SITE LPC CONF: LEXNET PVTs AT LL, ISI; PRNET AT SRI					

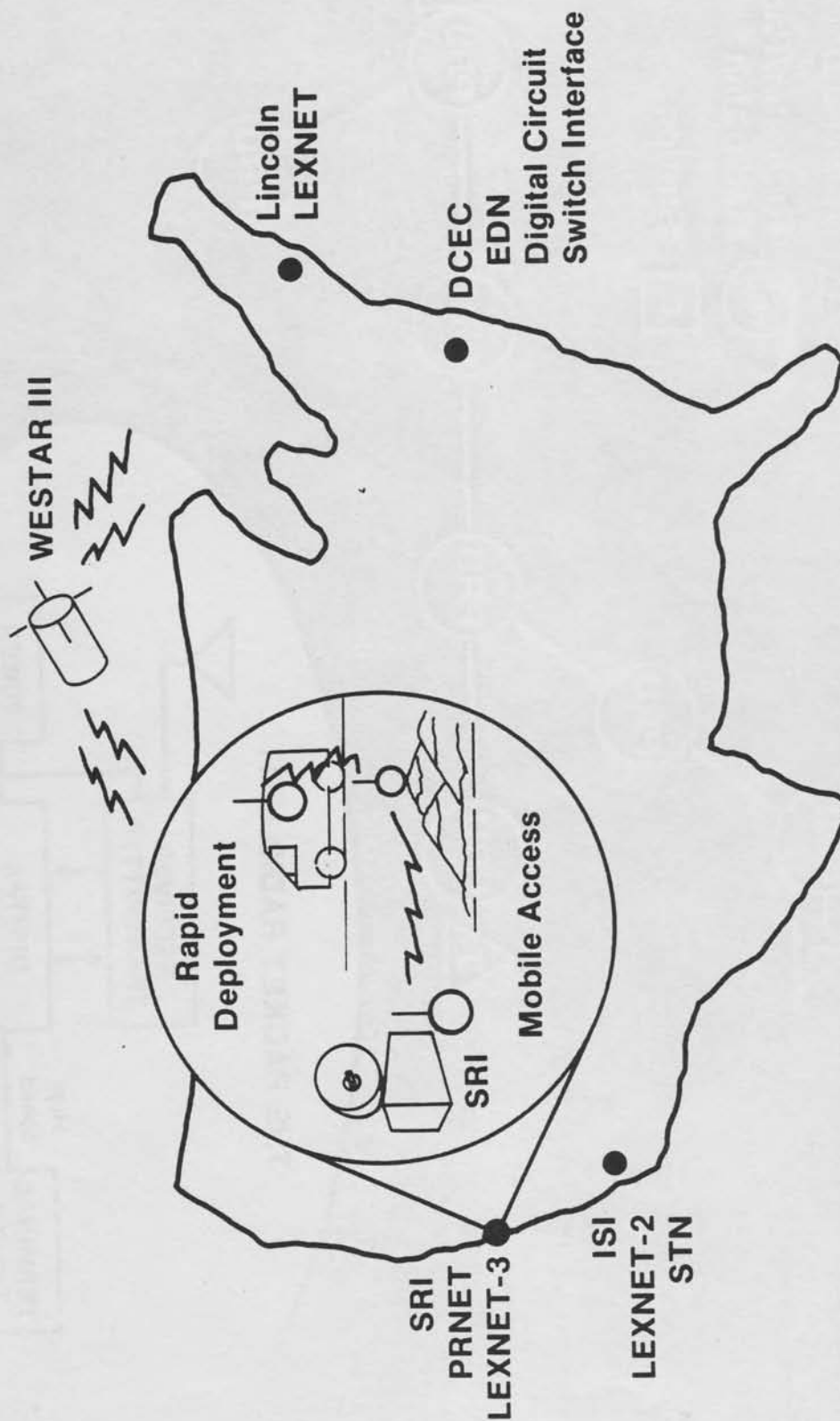
FUTURE DIRECTIONS

- MULTI-USER, MULTI-SITE EXPERIMENTS
 - MULTIPLEXING TO TEST SYSTEM LIMITS
 - ADAPTIVE TRAFFIC CONTROL OF VOICE AND DATA
 - INTERNET VOICE CONFERENCING
 - VOICE-CONTROLLED SYSTEMS
- PACKET VIDEO DEVELOPMENT/EXPERIMENTS
- SECURE PACKET SPEECH SYSTEM DEVELOPMENT/EXPERIMENTS

PACKET RADIO SPEECH

EARL J. CRAIGHILL
SRI INTERNATIONAL

EXPERIMENTAL WIDEBAND VOICE/DATA SATELLITE NETWORK



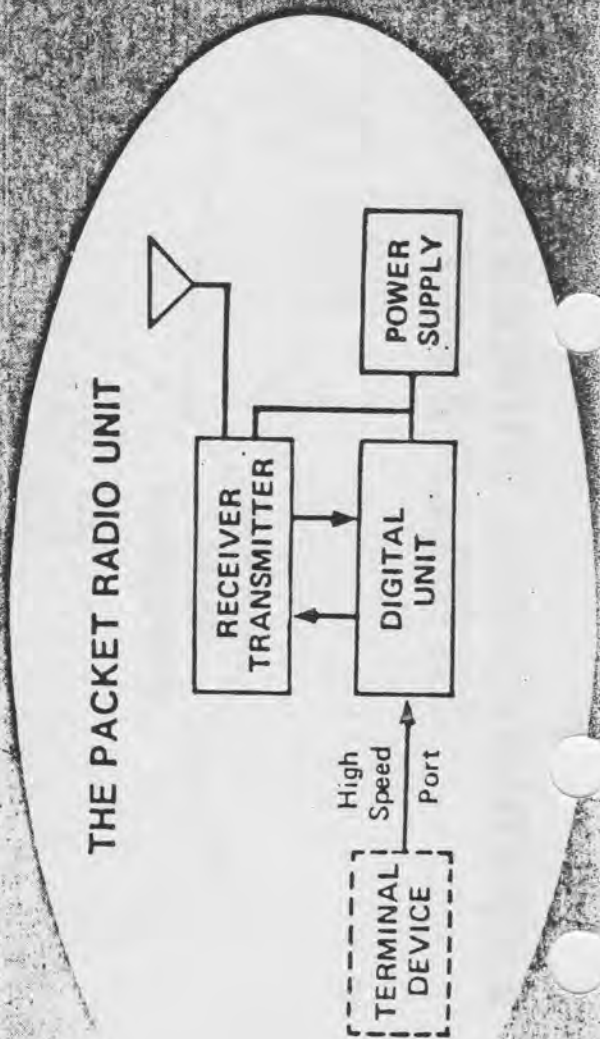
FEATURES

- Multiuser Voice/Data
- Satellite/Terrestrial
- Distributed Control
- Internet/Security Protocols
- Mobile Access for Voice
- Flexibility for Experiments

Subsystems at Each Satellite Net Node

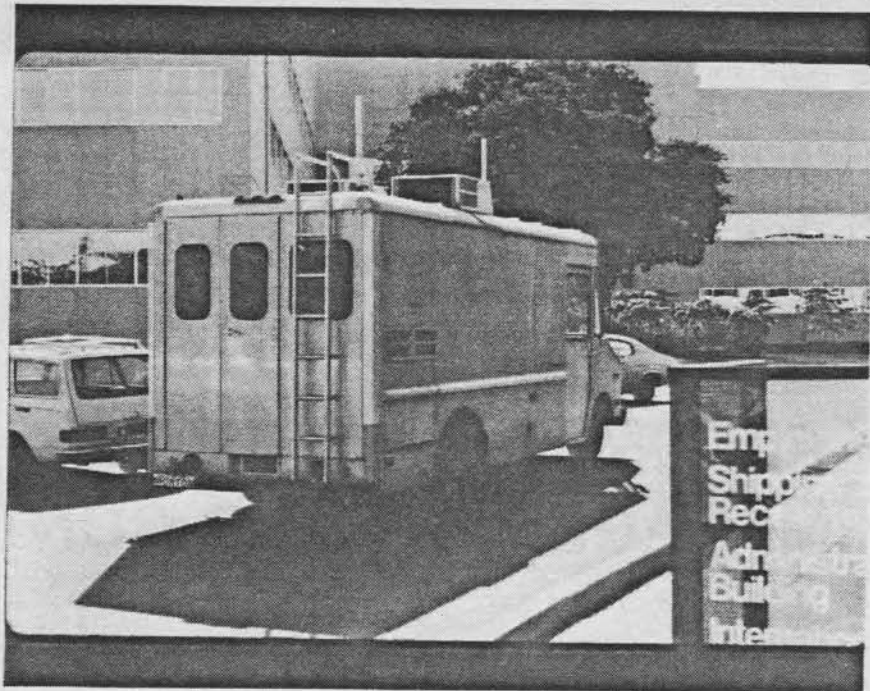
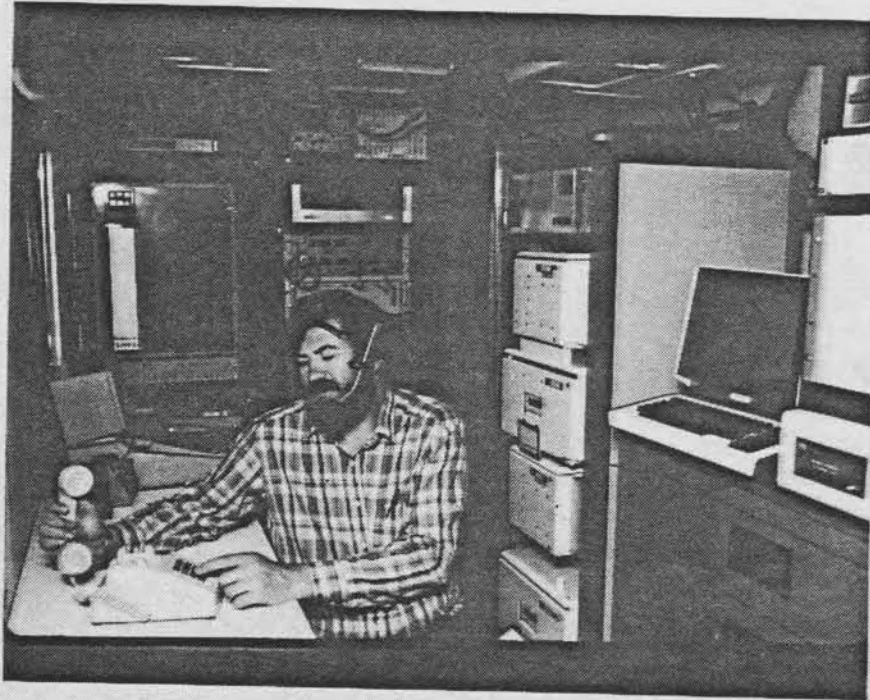
- Earth Station (RF)
- Flexible Burst Modem
- Demand Assignment Processor

THE PACKET RADIO UNIT (PRU) THE COMMON NETWORK ELEMENT

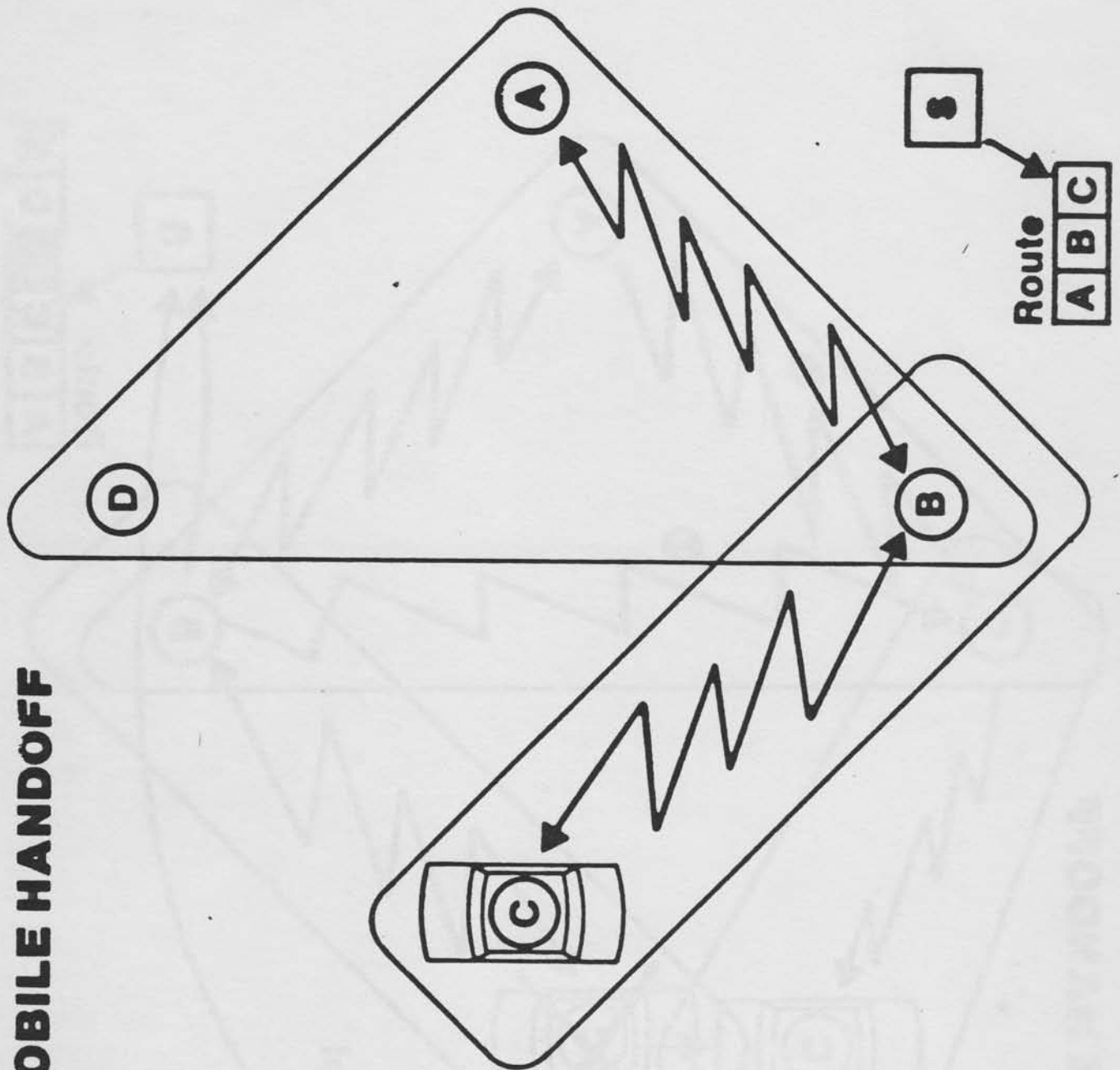


PACKET RADIO CONCEPTS

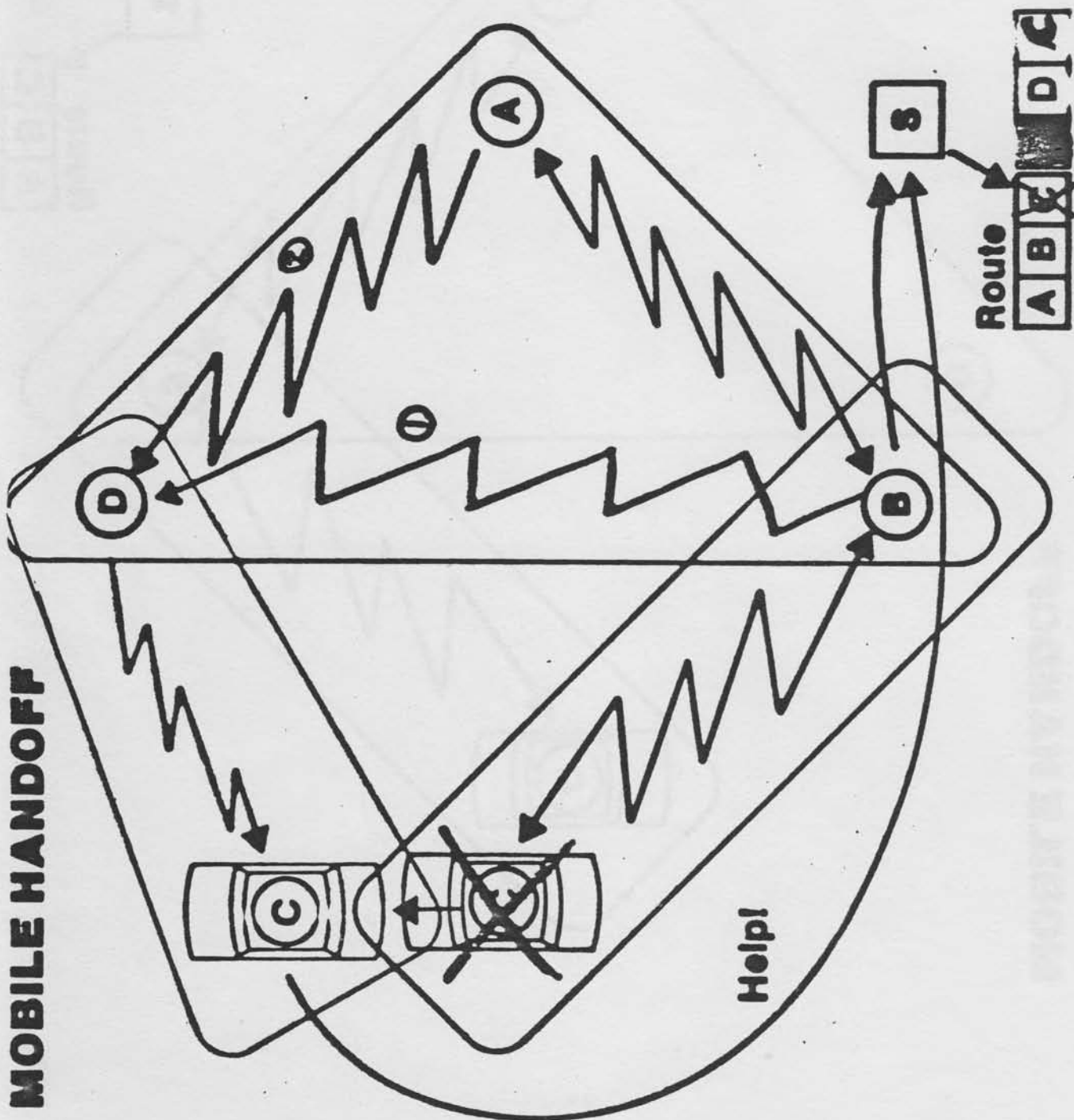
- **BROADCAST RADIO**
- **PACKET-SWITCHED**
- **MULTIPLE ACCESS**
- **MULTIPLE-HOP**
- **MOBILE OPERATION**
- **AUTOMATED NETWORK
MANAGEMENT AND CONTROL**



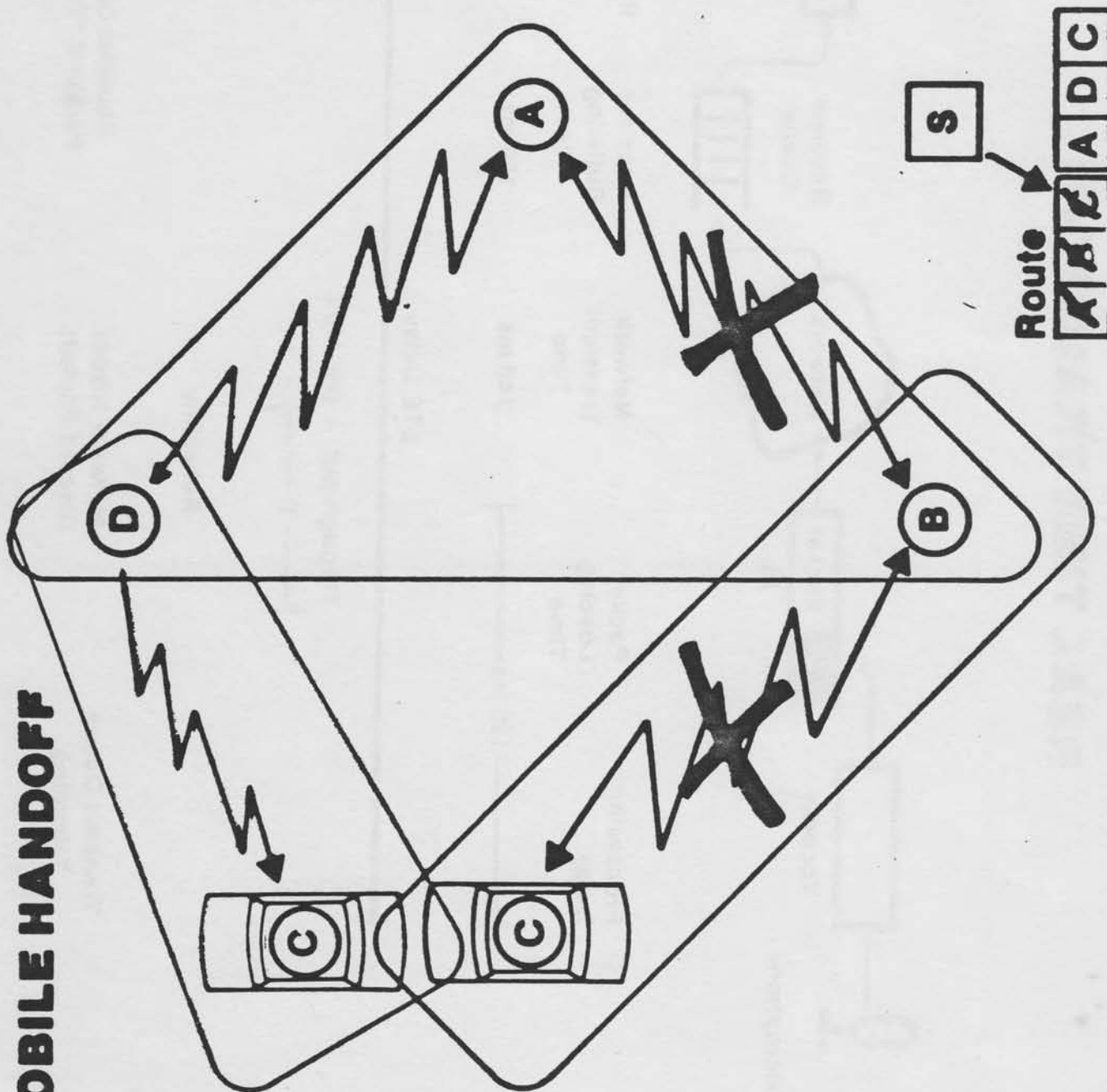
MOBILE HANDOFF



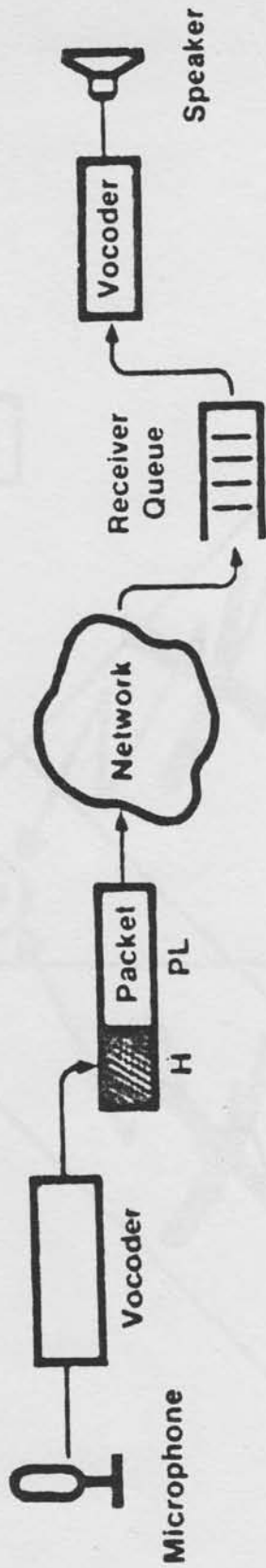
MOBILE HANDOFF



MOBILE HANDOFF



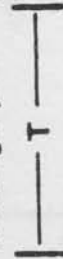
REAL TIME TRANSPORT



Processing Delay	Packet Loading Time	Network Transient Time	Receiver Buffering Time	Processing Delay
	135 ms	340 ms	150 ms	5 ms

ETE Delay

$$\text{Through put} = (PL-H)/T$$



Reliability

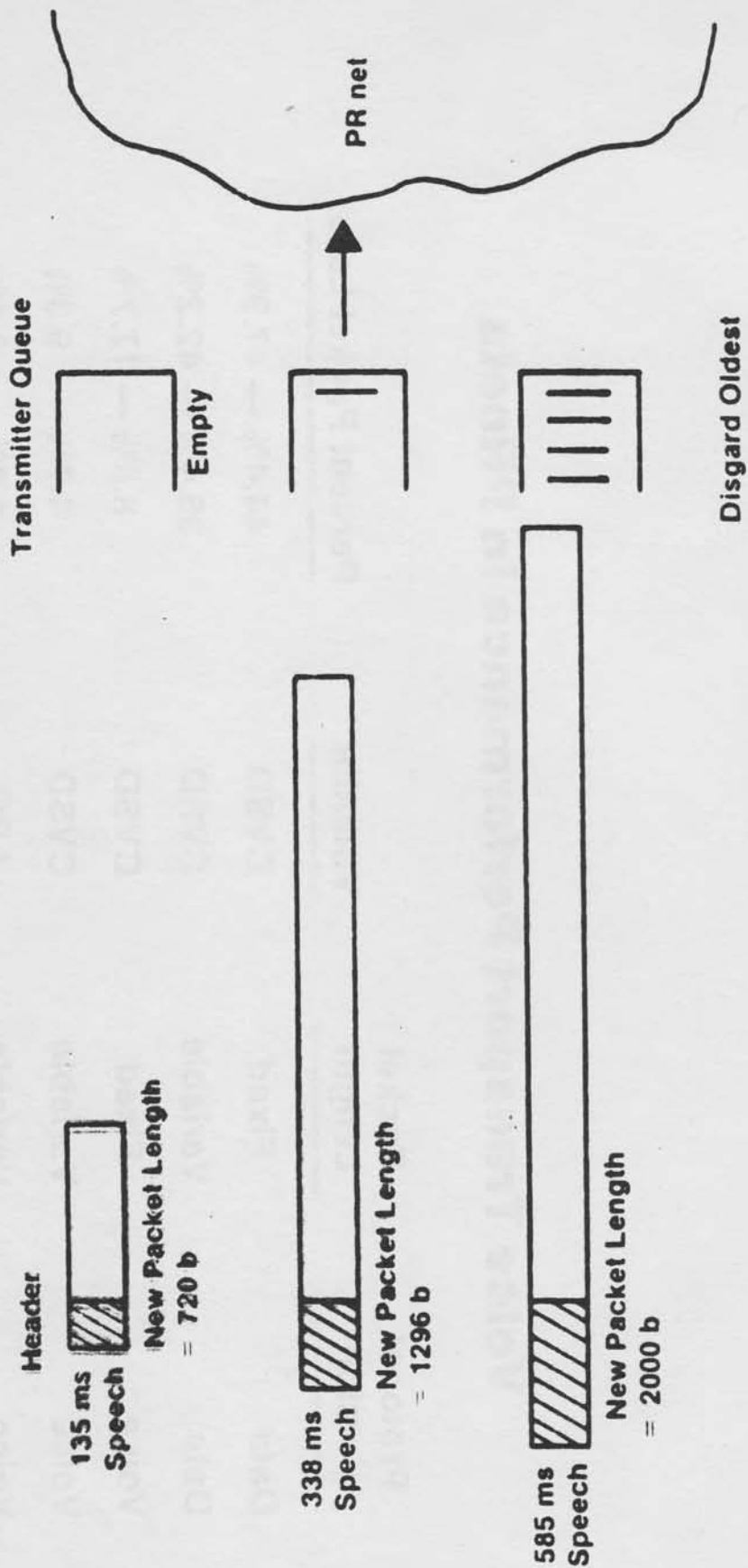
Transmit Queue Trimming

Network Nodes Discard Packets

Receiver Discards Packet if "Too Late"

TRANSMITTER FLOW CONTROL

Variable Packet Length
Controls the offering rate of packets to the network



Voice Transport Performance in PRnets

Protocol Version	Packet Length	Vocoder	Percent Packet Loss
Data	Fixed	CVSD	44.4% — 47.9%
Data	Variable	CVSD	35.4% — 42.2%
Voice	Fixed	CVSD	8.6% — 17.7%
Voice	Variable	CVSD	4.7% — 9.3%
Voice	Variable	LPC	1.8% — 3.1%

Need Type of Service to Support Data/Voice on the Same Network

- Different Requirements for Data and Voice
- Network Transport Parameters Changed on a Packet-by-Packet Basis
- Adjustments for Dynamic Network Conditions

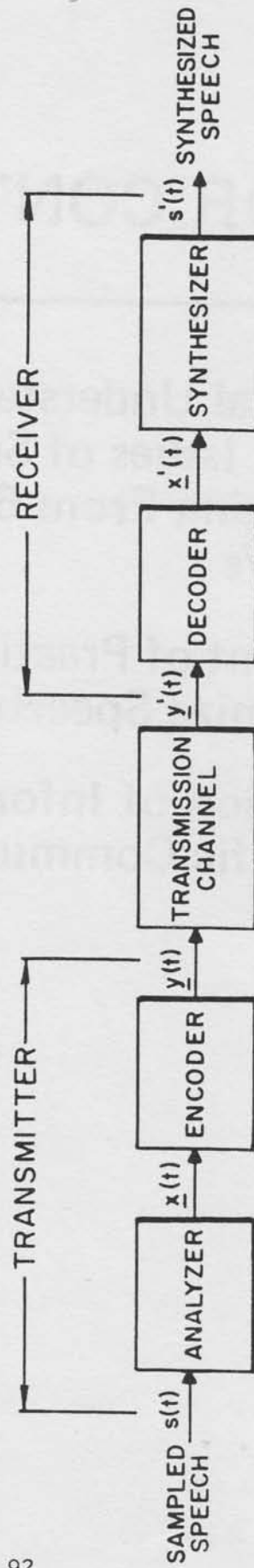
ALGORITHMIC ACHIEVEMENTS

JOHN MAKHOUL,
VISHU VISWANATHAN
BOLT BERANEK AND NEWMAN INC.

MAJOR CONTRIBUTIONS

- Fundamental Understanding of the Basic Theoretical Issues of Speech Coding at Data Rates Ranging From 64,000 bits/s Down to 100 bits/s
- Development of Practical Coding Algorithms That Maximize Speech Quality and Intelligibility
- Dissemination of Information to DoD Agencies and Scientific Community at Large

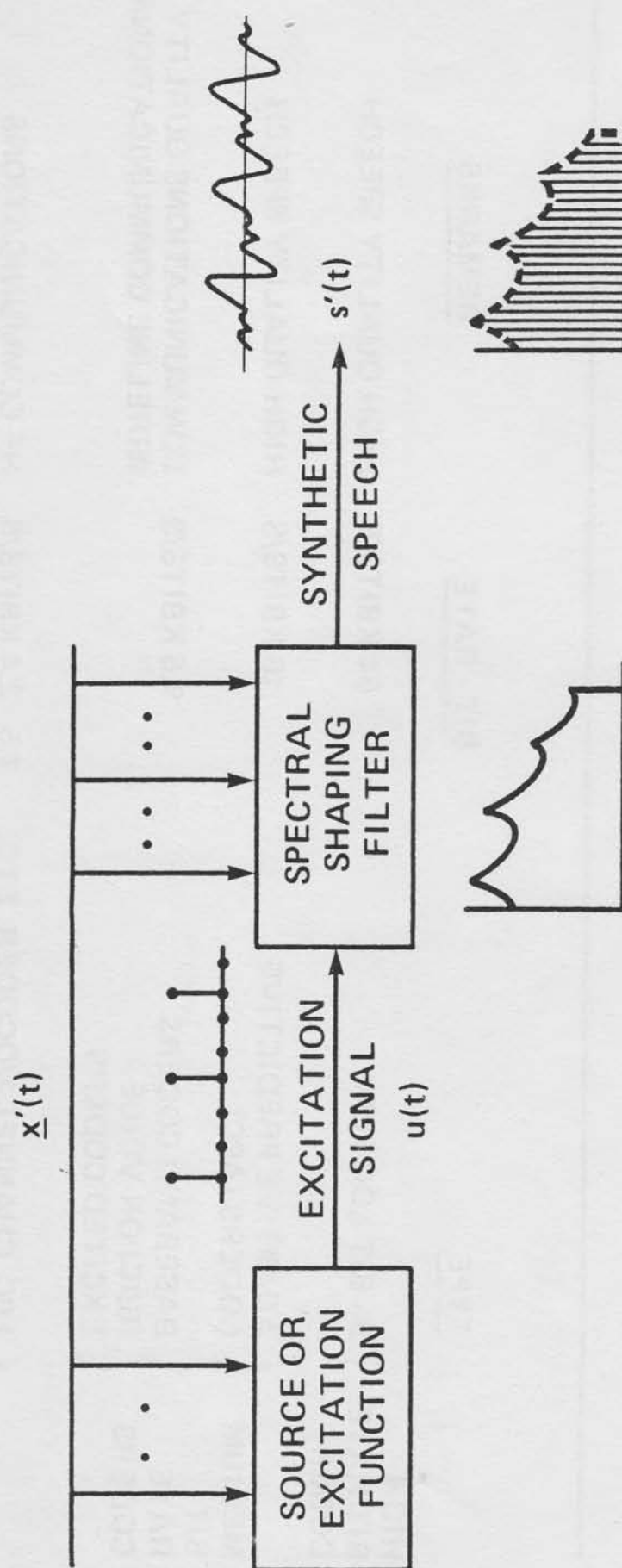
COMPONENTS OF A SPEECH COMPRESSION SYSTEM



TYPES OF SPEECH CODERS

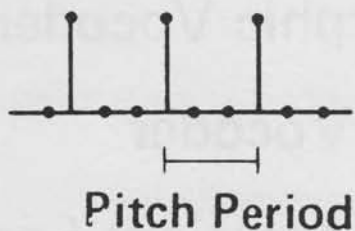
	<u>TYPE</u>	<u>BIT - RATE</u>	<u>REMARKS</u>
HIGH BIT RATE CODER	{ 8 - BIT LOG PCM	64 KBITS/S	HIGH QUALITY SPEECH
MEDIUM BIT RATE CODERS	{ ADAPTIVE PREDICTIVE CODERS (APC) BASEBAND CODERS (BBC) OR VOICE - EXCITED CODERS	16 KBITS/S 9.6 KBITS/S	HIGH QUALITY SPEECH COMMUNICATIONS QUALITY, WIRELINE COMMUNICATIONS
LOW BIT RATE CODERS	{ LPC, CHANNEL VOCODER, ETC. VECTOR QUANTIZATION SEGMENT VOCODER	1.5 - 2.4 KBITS/S 400 - 800 BITS/S 150 - 300 BITS/S	HF COMMUNICATIONS NAVY AND MINING SYSTEM APPLICATIONS LOW TRANSMISSION POWER.

A GENERAL SYNTHESIS MODEL



SOURCE MODELS FOR LOW BIT RATE VOCODERS

1. Pulse/Noise Model



Pulse Source for Voiced Sounds



Random Noise for Unvoiced Sounds

- Developed Robust Pitch and Voicing Extraction Algorithms
- Model too Idealized for Certain Sounds — Buzzy Speech Quality

2. Mixed-Source Model

- Uses Pulse and Noise Sources Simultaneously
- Eliminates Buzzy Quality and Produces More Natural-Sounding Speech
- Application in Phonetic Synthesis and Text-to-Speech Systems

SPECTRAL MODELS

- Linear Prediction (All-Pole) Model: LPC Vocoder
- Filter-Bank Model: Channel Vocoder
- Cepstral Model: Homomorphic Vocoder
- Formant Model: Formant Vocoder
- Spectral Amplitude Representation: Spectral Envelope Estimation Vocoder
- Pole-Zero Model

WHAT WE LEARNED:

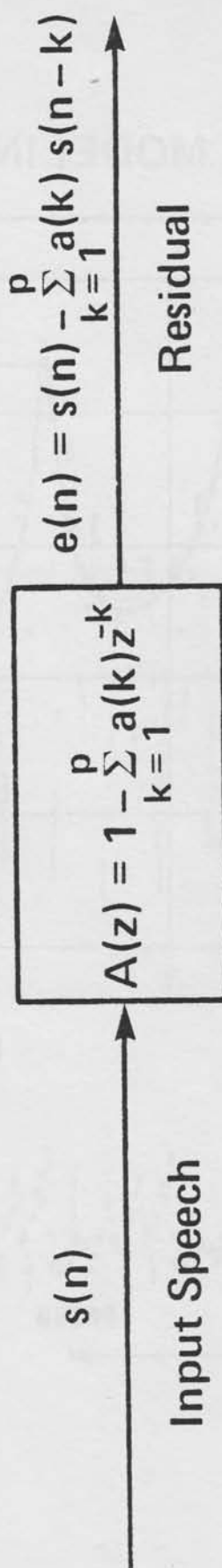
An Accurate Representation of the Short-Term Speech Spectral Envelope, Especially at Spectral Energy Peaks, Is Necessary for Good-Quality Speech Synthesis

LINEAR PREDICTION

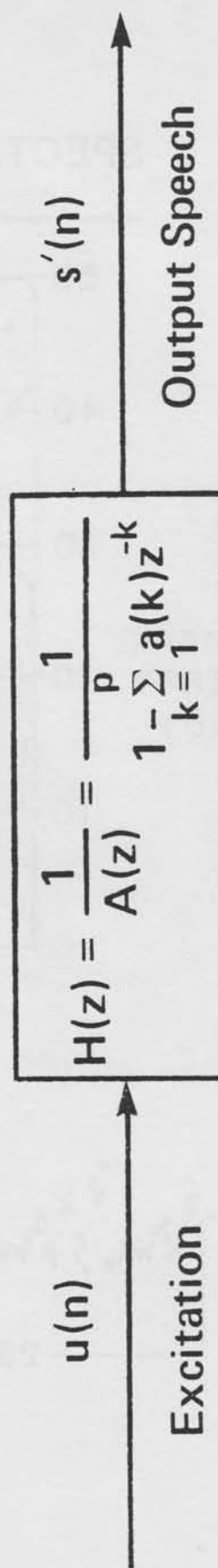
Each Speech Sample is Approximated by a Weighted Linear Summation of Previous Speech Samples:

$$s(n) \approx \sum_{k=1}^p a(k) s(n-k).$$

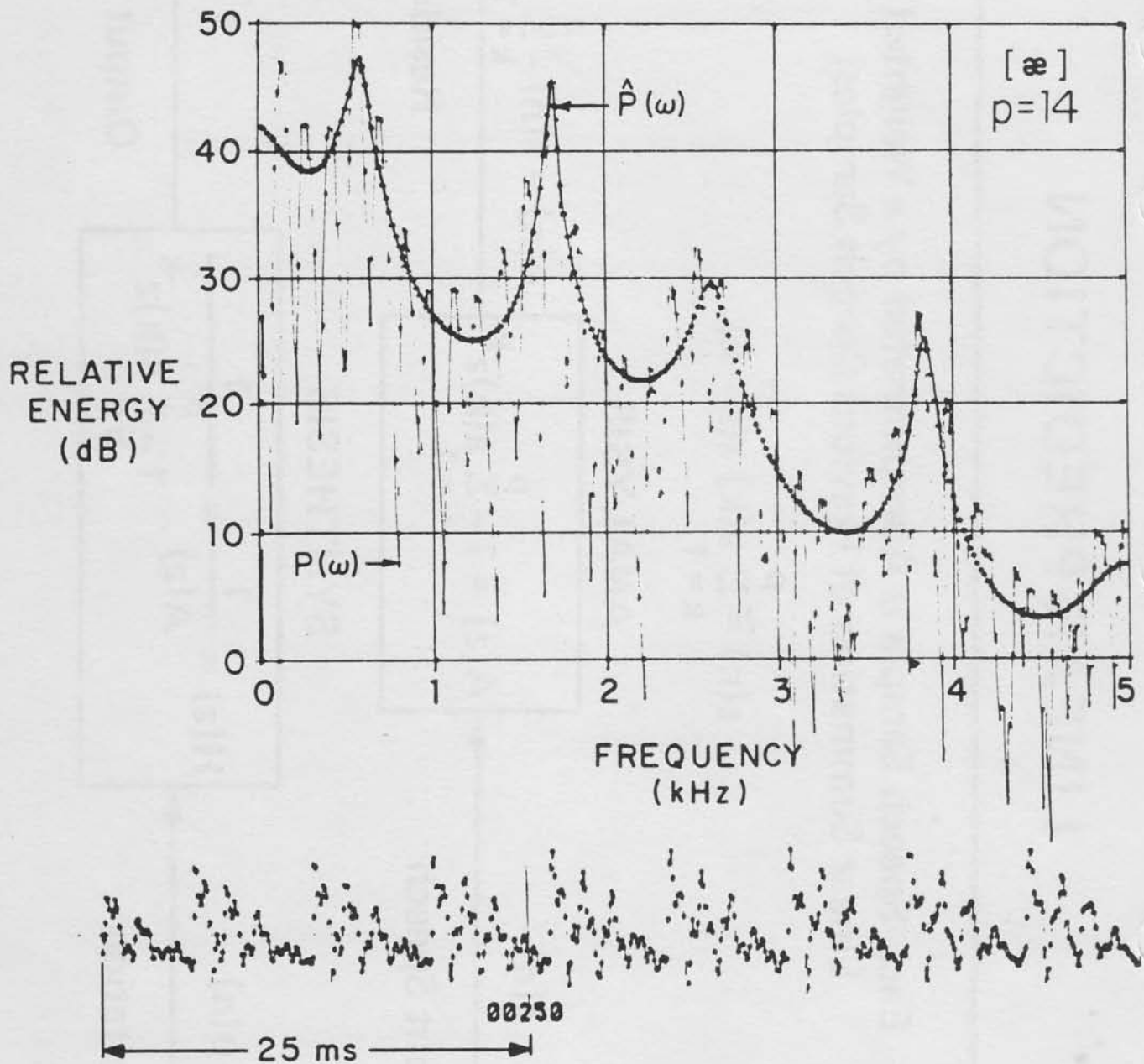
ANALYSIS



SYNTHESIS



SPECTRAL MODELING BY LINEAR PREDICTION

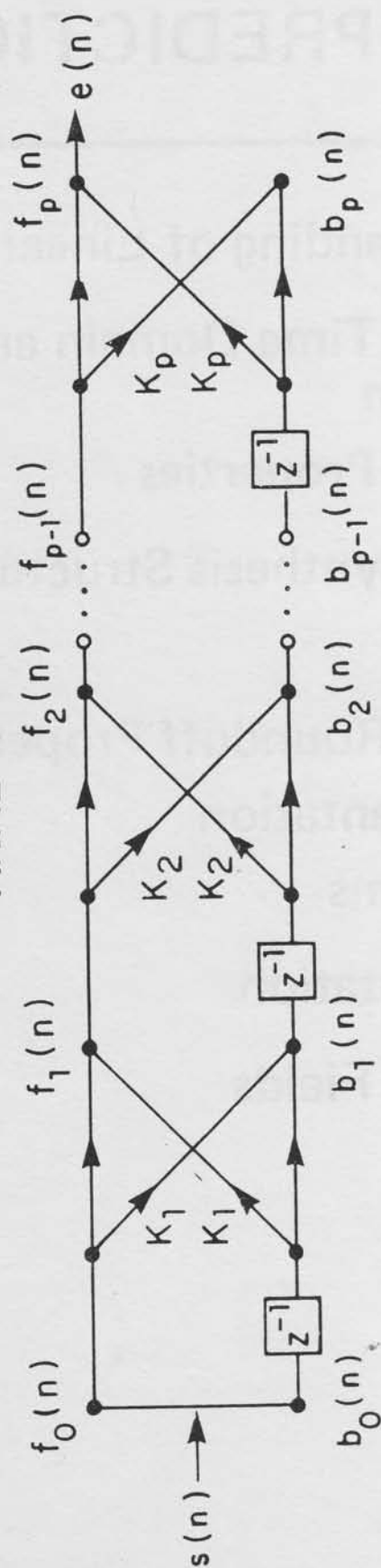


CONTRIBUTIONS IN LINEAR PREDICTION

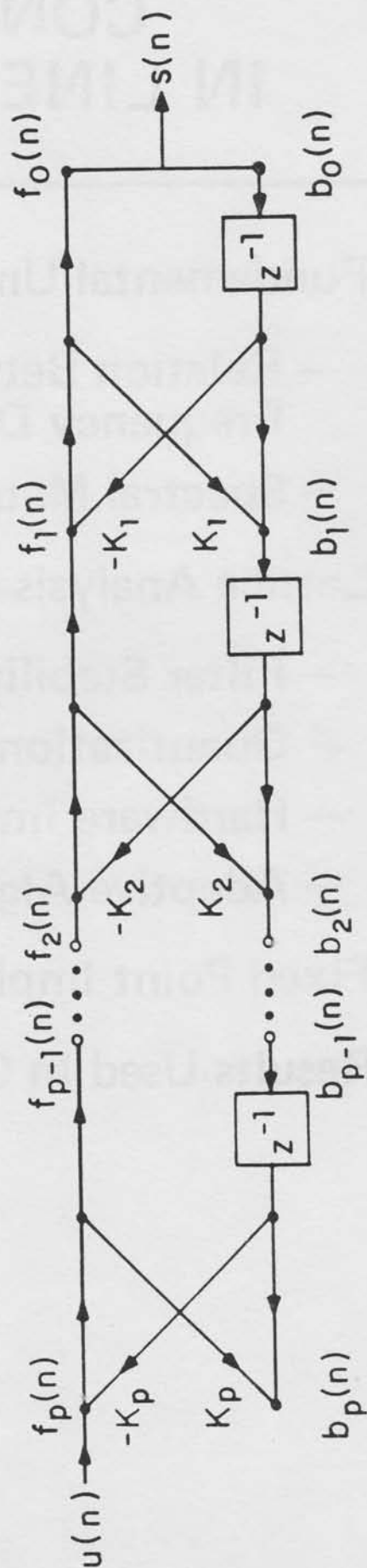
1. Fundamental Understanding of Linear Prediction
 - Relation Between Time Domain and Frequency Domain
 - Spectral Matching Properties
2. Lattice Analysis and Synthesis Structures
 - Filter Stability
 - Quantization and Roundoff Properties
 - Hardware Implementation
 - Adaptive Algorithms
3. Fixed-Point Implementation
4. Results Used In Other Fields

LATTICE METHODS

ANALYSIS

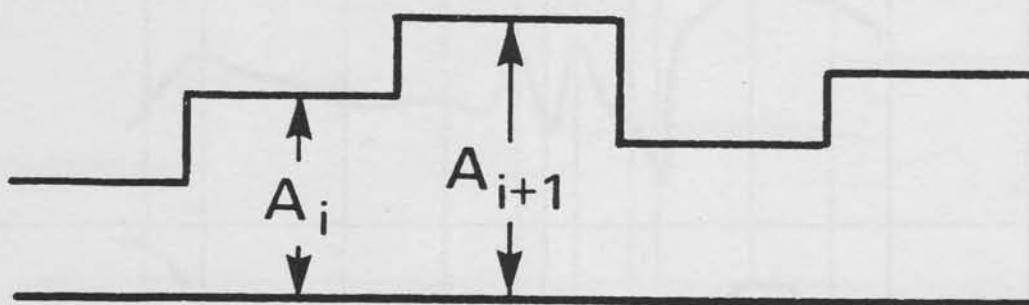


SYNTHESIS



QUANTIZATION OF SPECTRAL PARAMETERS

- Quantization Properties of Different Parametric Representations
 - Reflection Coefficients $\{K_i\}$
- The Notion of Spectral Sensitivity for Optimal Quantization
 - Log Area Ratios $\{L_i\}$
 - Arc Sine Parameters



VOCAL TRACT MODEL

$$L_i = \log \frac{A_{i+1}}{A_i} = \log \frac{1+K_i}{1-K_i}$$

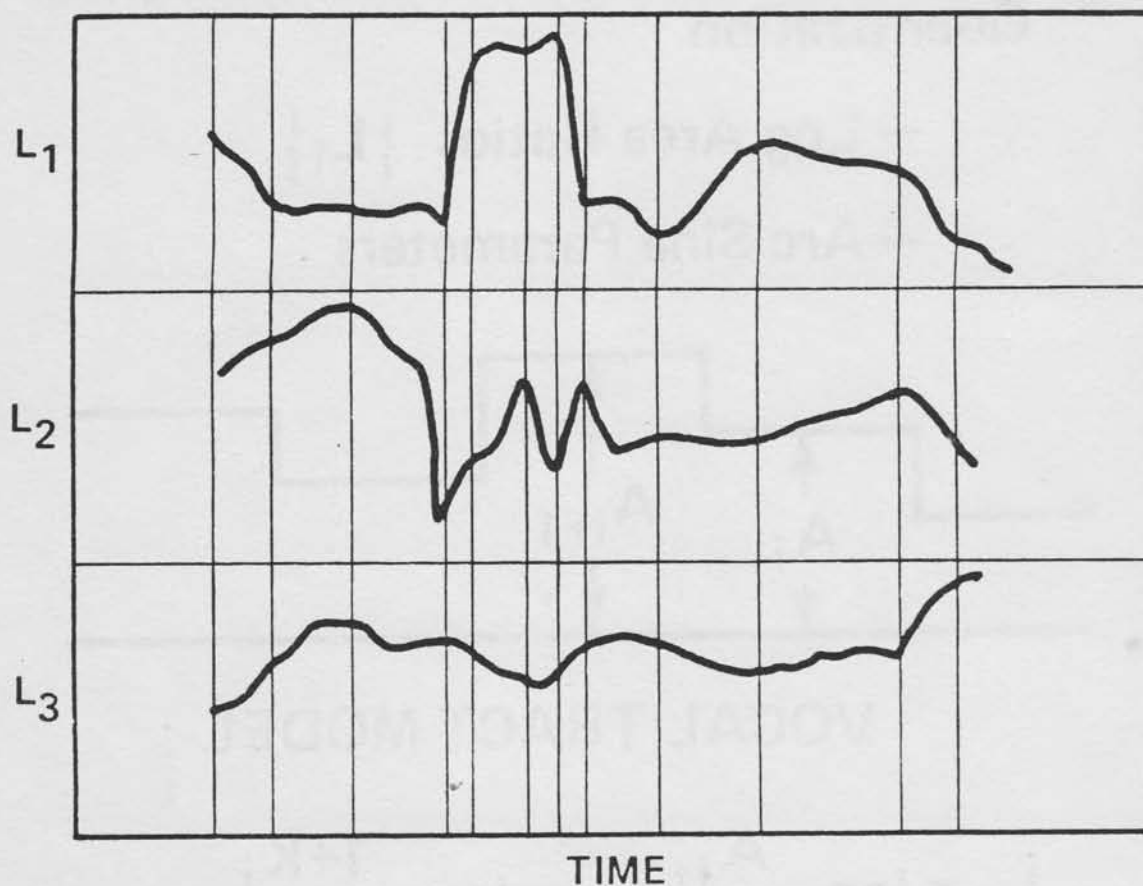
VARIABLE FRAME RATE TRANSMISSION

IDEA:

- Coder Parameters Are Transmitted Only if They Have Changed Sufficiently Since the Last Transmission

METHOD:

- Transmit Selected Frames of Parameters, with the Selection Made Independently for Pitch, Gain and Spectral Parameters
- Reconstruct the Untransmitted Parameters by Linear Interpolation



VARIABLE FRAME RATE TRANSMISSION-RESULTS

	<u>Bits/s</u>
1. Fixed Frame Rate	
100 Frames/s	5600
2. Variable Frame Rate	
Average: 31 Frames/s	2075

RESULT:

Systems 1 and 2 Produce the Same
Speech Quality

ROBUST PERFORMANCE UNDER ACOUSTIC BACKGROUND NOISE

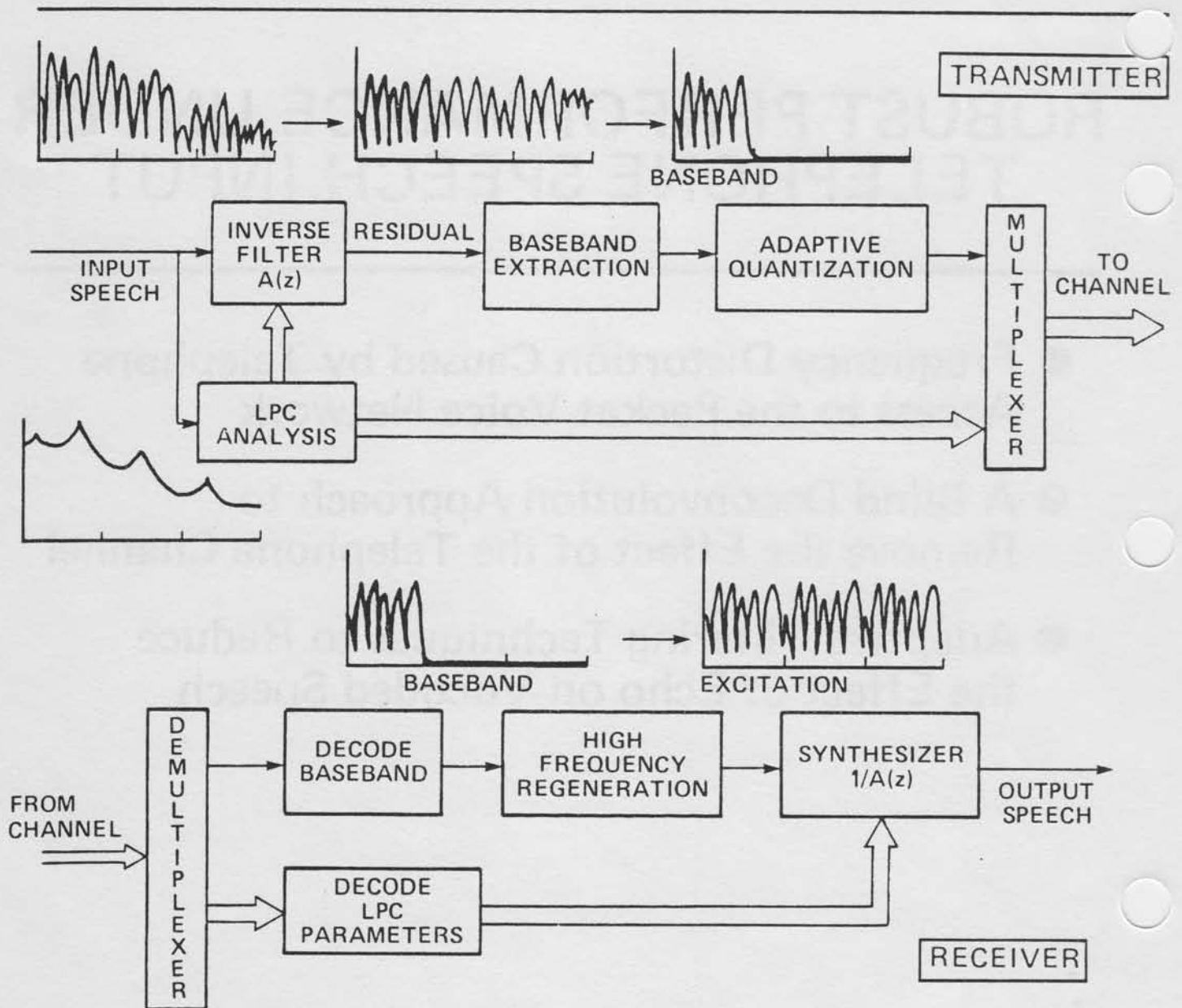
THREE APPROACHES:

1. Noise-Cancelling Microphones (Sponsored by Other DoD Agencies)
2. Two-Microphone Input for Adaptive Noise Cancelling
3. Single Microphone Input
 - Preprocessing by Spectral Subtraction Method
 - Preprocessing Enhances the Quality and Intelligibility of Vcoded Speech in Acoustic Background Noise

ROBUST PERFORMANCE UNDER TELEPHONE SPEECH INPUT

- Frequency Distortion Caused by Telephone Access to the Packet Voice Network
- A Blind Deconvolution Approach to Remove the Effect of the Telephone Channel
- Adaptive Filtering Techniques to Reduce the Effect of Echo on Vcoded Speech

MEDIUMBAND SPEECH CODING



MULTIRATE SPEECH CODING

- Transmission at a Wide Range of Bit Rates to Accommodate Varying Traffic Loads on the Packet Network
- Embedded-Code Systems
- Specific Designs Considered:
 - CVSD/PCM (16 to 64 kbits/s)
 - LPC Vocoder/Adaptive Transform Coder (2.4 to 16 kbits/s)
 - Channel Vocoder/Sub-Band Coder (2.4 to 9.6 kbits/s)

LOW BIT RATE VOCODERS

1. Scalar Quantization of Spectral Parameters (1.5-2.4 kbits/s)
 - Independent Quantization of Each Parameter
2. Vector Quantization of Spectral Parameters (400-800 bits/s)
 - Parameters Quantized as a Vector in Multi-Dimensional Space
 - Use Clustering to Determine Quantization Templates
3. Segment Quantization (150-300 bits/s)
 - Quantize a Sequence of Spectra as One Unit
4. Phonetic Vocoder (100 bits/s)
 - Use Speech Recognition Techniques

STATE-OF-THE-ART IN SPEECH COMPRESSION

- Virtually Transparent Speech Quality at 16 kbits/s
- Quality and Intelligibility Degrade With Decreasing Bit-Rate, Especially
 - Below 4.8 kbits/s
 - For Female Speech
 - Under Acoustic Noise and Channel Distortion Conditions
- Substantially Improved Intelligibility and Quality of 2.4 kbits/s Vocoder

AREAS OF FURTHER RESEARCH

PROBLEM: How to Maximize Speech Quality and Intelligibility for Every bit That We Use in Transmission?

- Source Modeling
 - Pitch and Voiced/Unvoiced Decision
- Spectral Modeling
 - Female Speech
- Pattern Recognition and Information Theoretic Coding Techniques
- Understanding and Modeling of the Effects of Coding Techniques on Human Speech Perception

VERY LOW RATE VOCODER

RICHARD SCHWARTZ
BOLT BERANEK AND NEWMAN INC.

VERY LOW RATE VOCODER

- Requirements

- 100-200 bits/s
- Intelligibility in a Conversation
- Naturalness

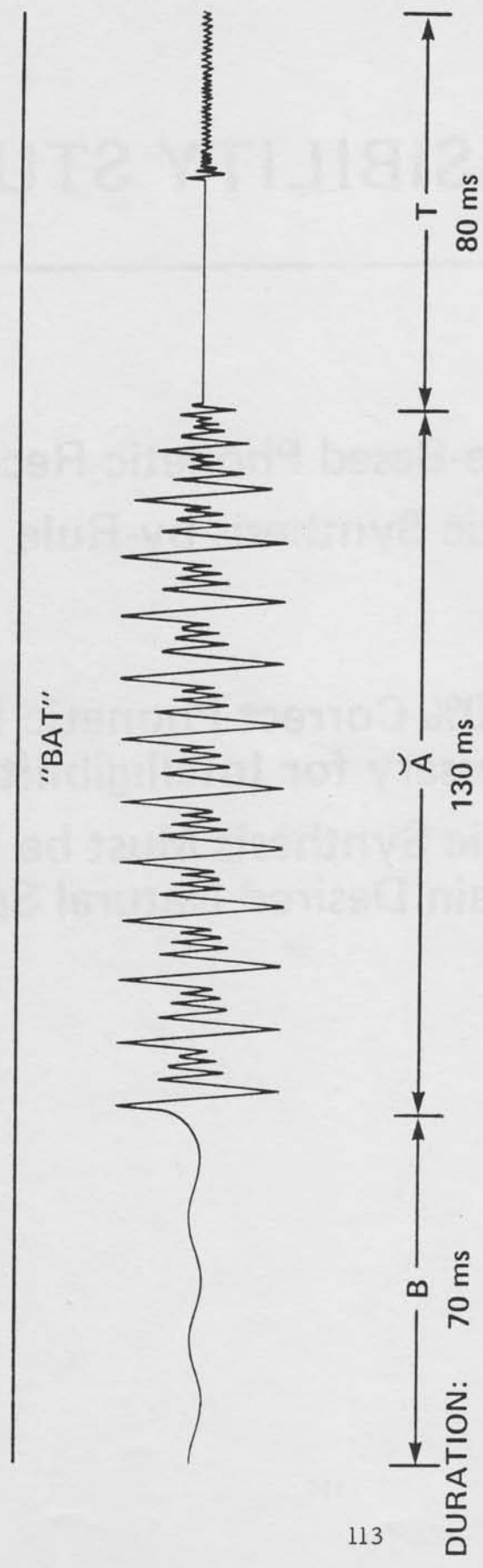
- Applications

- Low Power Communication
- Degraded Channel Conditions
- "Burn Through" Jamming Networks
- Speech Storage

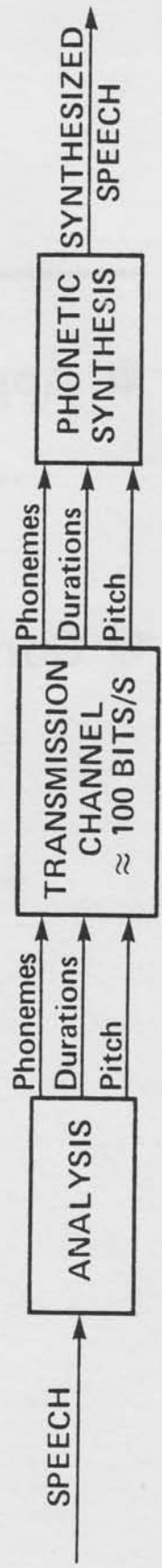
VERY LOW RATE VOCODERS

1. Phonetic Vocoder ~100 bits/s
2. Segment Vocoder ~150-300 bits/s

PHONETIC VOCODER



Number of Phonemes in English: 42
 Typical Speaking Rate: 12 Phonemes/sec.



FEASIBILITY STUDY

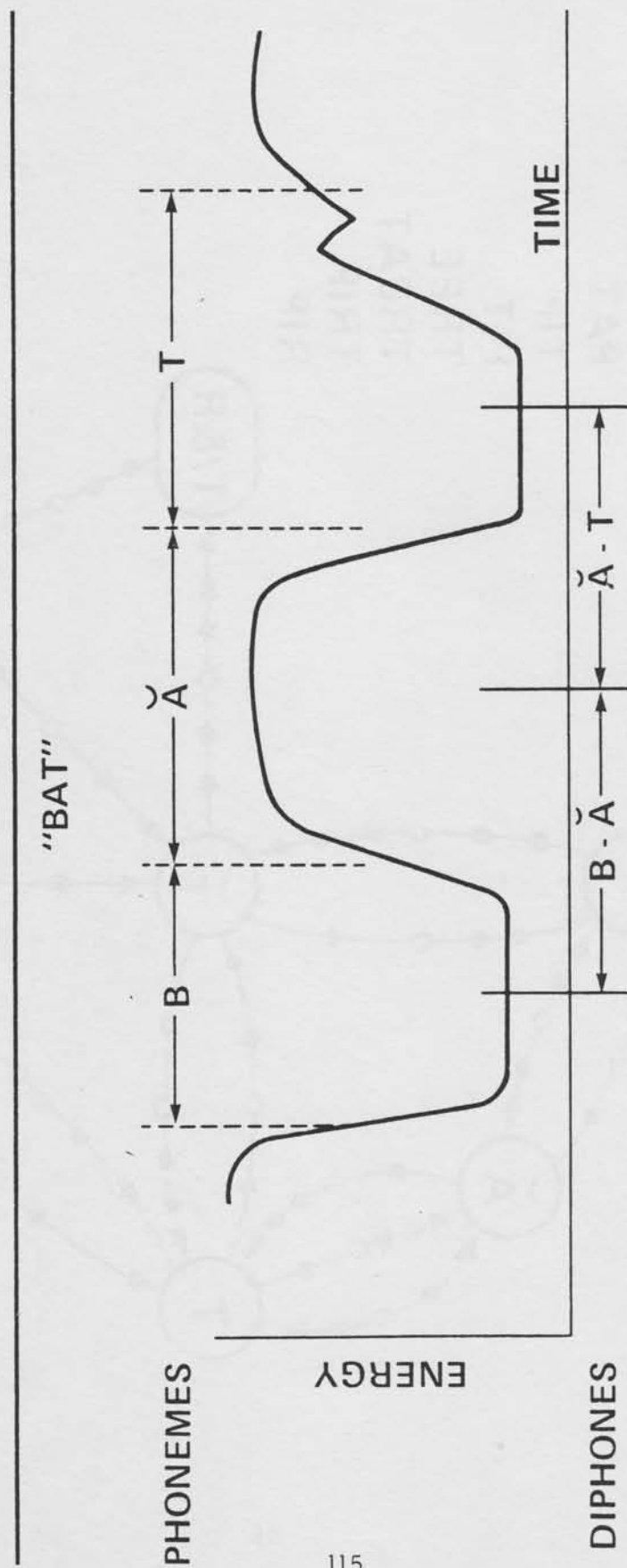
- Approach

- Feature-Based Phonetic Recognition
- Phonetic Synthesis-by-Rule

- Conclusions

- Over 80% Correct Phonetic Recognition Is Necessary for Intelligibility in Context
- Phonetic Synthesis Must be Improved to Obtain Desired Natural Speech Quality

DIPHONE SYNTHESIS

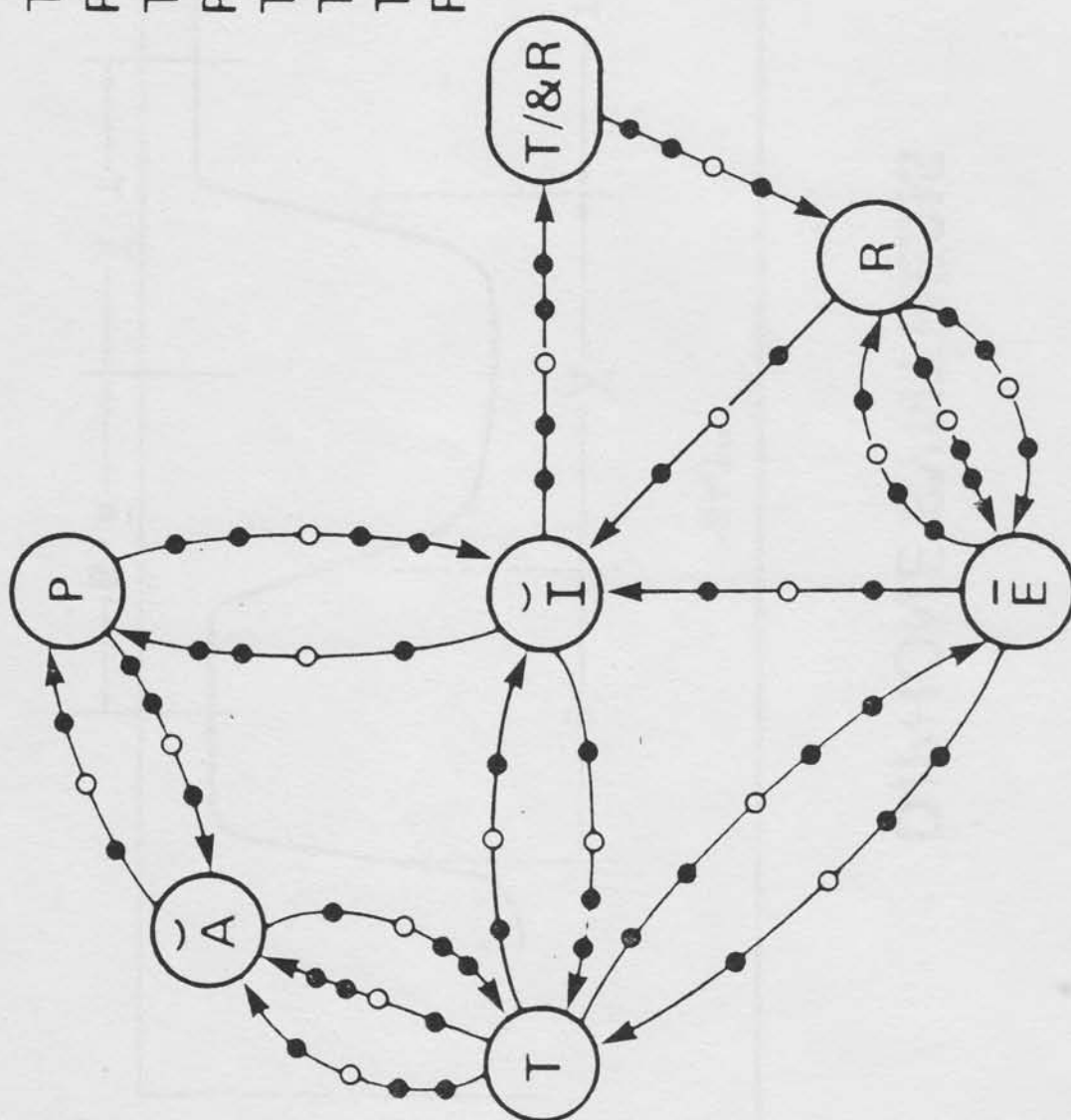


SPEECH IS SYNTHESIZED BY CONCATENATING DIPHONE TEMPLATES

DIPHONE RECOGNITION NETWORK

TAP = T Ä P

PAT
TIP
PIT
TREE
TREAT
TRIP
RIP



PHONETIC VOCODER

- Requires Phonetic Recognition
 - Still a Difficult Problem
- Requires Manual Labeling of Diphones
 - Labor Intensive

SEGMENT VOCODER

- A Segment Is a “Diphone-Like” Sequence of Spectra Between Two Steady State Sounds
- Segment Templates Are Selected Automatically (Unsupervised)
 - There Is No Phonetic Labeling
- Result: Segment Vocoder Speech Is Intelligible at About 150 bits/s

AUTOMATIC TEMPLATE SELECTION

- Training Data: 15 Minutes of Unconstrained Speech
- Segmentation Algorithm:
 - Divides Training Speech Into “Diphone-Like” Segments (15 Minutes Contains About 8,000 or 2^{13} Segments)
- Random Quantizer
 - All Segments are Used as Templates
- Template Network:
 - Determines Constraints on Template Sequences by Requiring Spectral Continuity Between Successive Templates
 - Only 1024 or 2^{10} Templates Can Follow Any Given Template

BIT ALLOCATION FOR SEGMENT VOCODER

	<u>Bits/Segment</u>
Segment Template Code	10
Segment Duration	1½
Pitch	1
Energy	1½
Total Bits/Segment	14
Average Segment Rate	11 per sec
Average Bit Rate = $11 \times 14 = 154$ bits/s	

PACKET VOICE TERMINALS
AND
THE LEXNET LOCAL NETWORK

GERALD C. O'LEARY
MIT LINCOLN LABORATORY

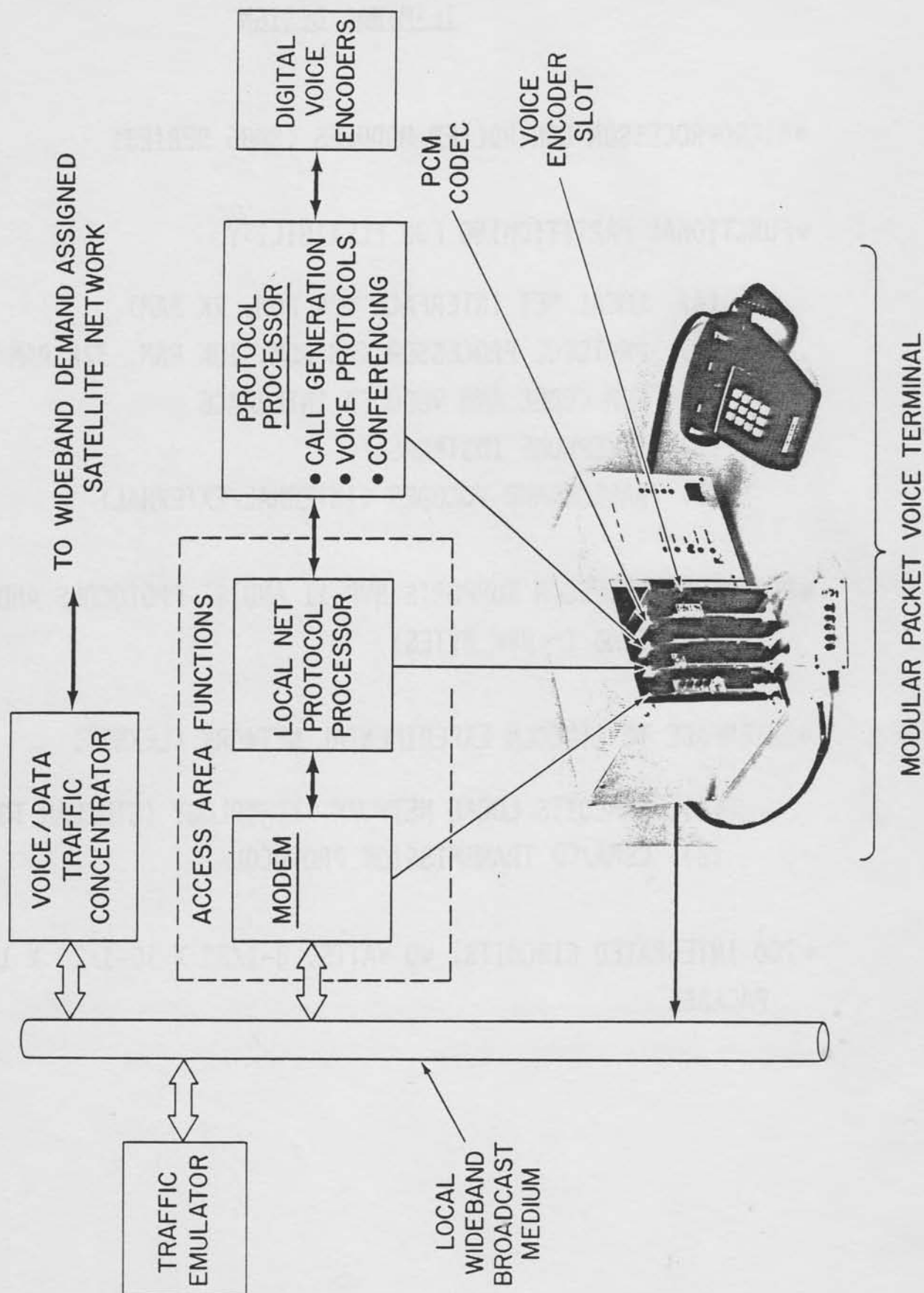
PACKET VOICE TERMINAL AND LEXNET

- PVT REQUIREMENTS
- ARCHITECTURE
- SPEECH PROCESSOR OPTIONS
- LEXNET
- CURRENT STATUS
- FUTURE DIRECTIONS

PACKET VOICE TERMINAL REQUIREMENTS

- ACCOMMODATE PCM AND NARROWBAND SPEECH PROCESSORS
- IMPLEMENT PACKET VOICE PROTOCOLS
- SUPPORT CONNECTION TO DIFFERENT PACKET NETS
- TELEPHONE-LIKE USER INTERFACE
- SOURCE OF PACKET SPEECH TRAFFIC FOR WIDEBAND PACKET VOICE EXPERIMENTS

LINCOLN EXPERIMENTAL PACKET VOICE NETWORK



TERMINAL DESIGN

- MICROPROCESSOR CONTROLLED MODULES (8085 SERIES)
- FUNCTIONAL PARTITIONING FOR FLEXIBILITY
 - (A) LOCAL NET INTERFACE (2K ROM, 2K RAM)
 - (B) PROTOCOL PROCESSOR (2K ROM, 10K RAM, 32K RAM/ROM)
 - (C) PCM CODEC AND VOCODER INTERFACE
 - (D) TELEPHONE INSTRUMENT
 - (E) NARROWBAND VOCODER (INTERNAL/EXTERNAL)
- PROTOCOL PROCESSOR SUPPORTS NVP-11 AND ST PROTOCOLS AND
CONFERENCING (~ 28K BYTES)
- INTERFACE TO LINCOLN EXPERIMENTAL NETWORK (LEXNET)
 - (A) EXPLOITS LOCAL NETWORK TECHNOLOGY (SIMILAR TO ETHERNET)
 - (B) CSMA/CD TRANSMISSION PROTOCOL
- 200 INTEGRATED CIRCUITS, 40 WATTS, 8-1/2" X 10-1/2" X 16-1/2"
PACKAGE

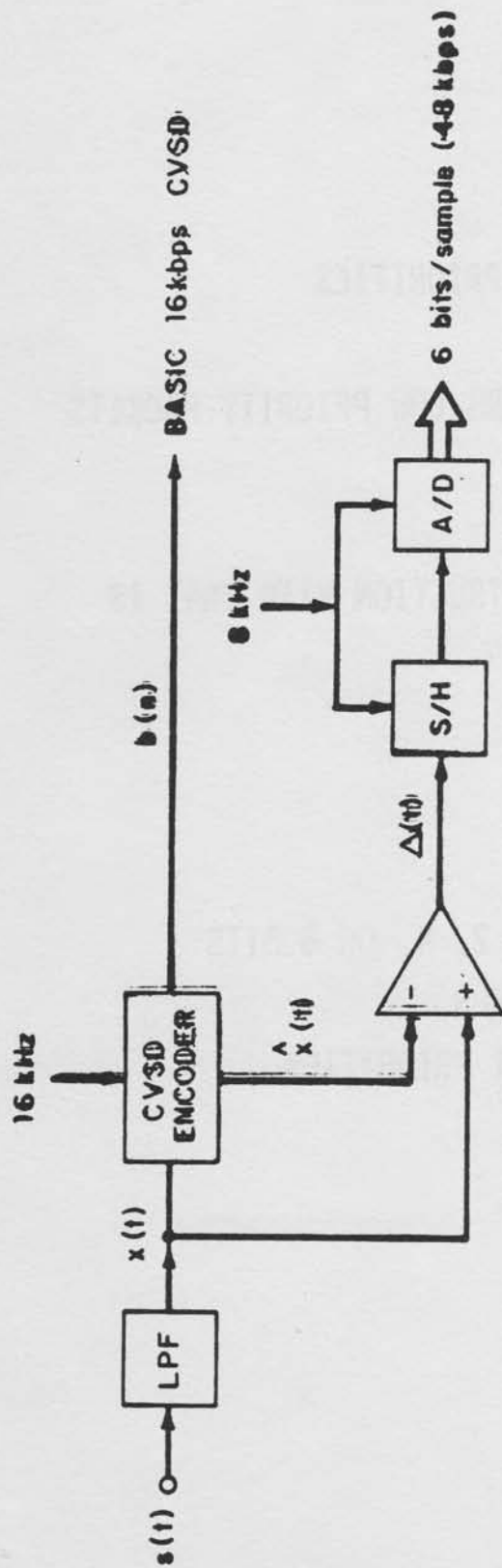


SPEECH PROCESSOR OPTIONS

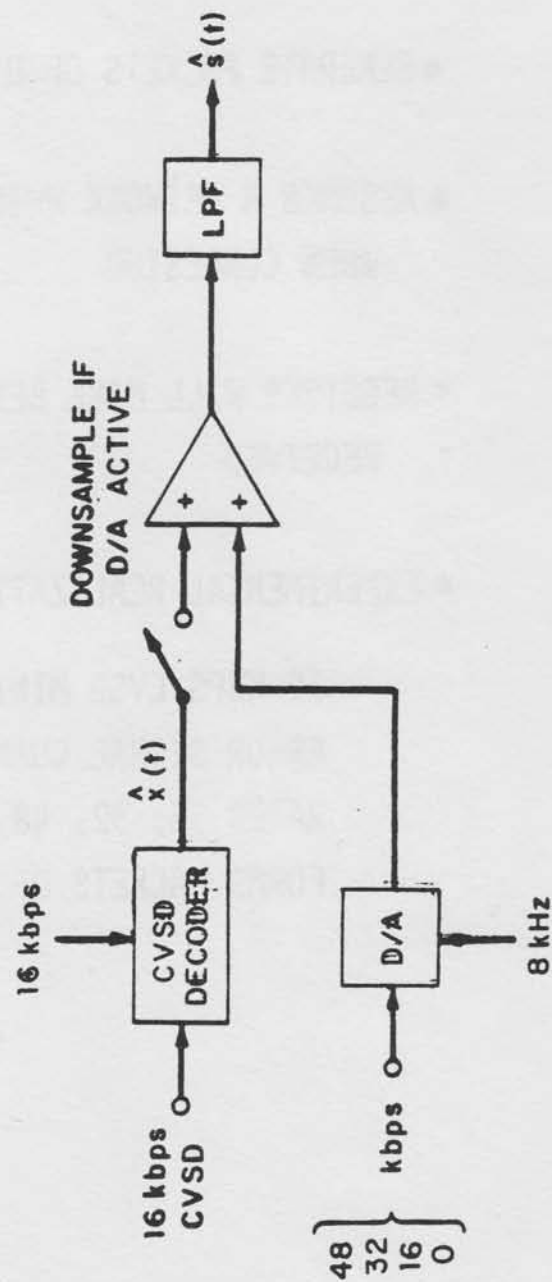
- 64 KBIT/SEC PCM
- 16 - 64 KBIT/SEC EMBEDDED CVSD
- 2400 BIT/SEC LPC
- SWITCHED TELEPHONE NETWORK INTERFACE CARD
- NETWORK TIMING MEASUREMENTS CARD

EMBEDDED VOCODER

- VARIABLE RATE VOCODER
- RATE-QUALITY TRADE-OFF
- GENERATE PACKETS OF DIFFERENT PRIORITIES
- ASSUMES A NETWORK WHICH DISCARDS LOW PRIORITY PACKETS WHEN CONGESTED
- RECEIVER WILL MAKE BEST RECONSTRUCTION WITH WHAT IS RECEIVED
- EXPERIMENTAL REALIZATION
 - 16 KBPS CVSD MINIMUM RATE
 - ERROR SIGNAL QUANTIZED TO 2, 4, OR 6 BITS
 - RATES 16, 32, 48, OR 64 KBPS
 - FORMS PACKETS OF DIFFERENT PRIORITIES



(a)



(b)

LINCOLN EXPERIMENTAL PACKET VOICE NETWORK (LEXNET)

- CONNECTS PVTs TO FORM DISTRIBUTED TELEPHONE SYSTEM
- CONCENTRATOR INTERFACE BOX PROVIDES HIGH RATE CONNECTION TO SATELLITE CHANNEL
- CONFERENCE ACCESS CONTROLLER
- LINCOLN'S NET SPANS ABOUT 1000 FEET
- 1 MBIT/SEC ON RG-59/U COAXIAL CABLE

SUMMARY

- CURRENT STATUS

NETWORKS AT LINCOLN (2),

ISI

SRI

DCEC

10 TERMINALS

- FUTURE DIRECTIONS

INTEGRATE PACKET VOICE CAPABILITY TO OTHER

DoD DATA NETWORKS

SECURE SPEECH TERMINALS

TECHNOLOGY TRANSFER

VOICE CONTROLLED CONFERENCE SET UP

NETWORK TIMING MEASUREMENTS

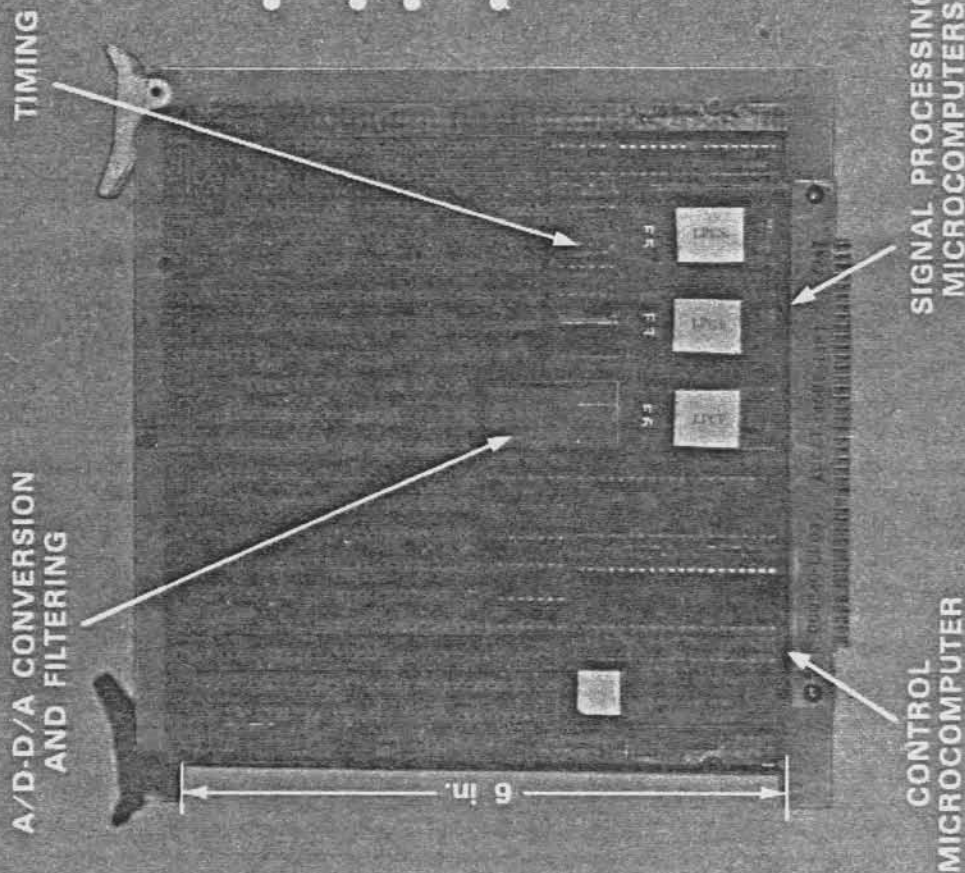
COMPACT LPC VOCODER

JOEL A. FELDMAN
MIT LINCOLN LABORATORY

PVT SINGLE BOARD 2.4 KBPS LPC VOCODER

- HARDWARE**
- ARCHITECTURE**
- PROCESSORS' TASKS**
- PROCESSORS' REAL-TIME AND MEMORY USAGE**
- INITIALIZATION OPTIONS**

COMPACT LPC VOCODER

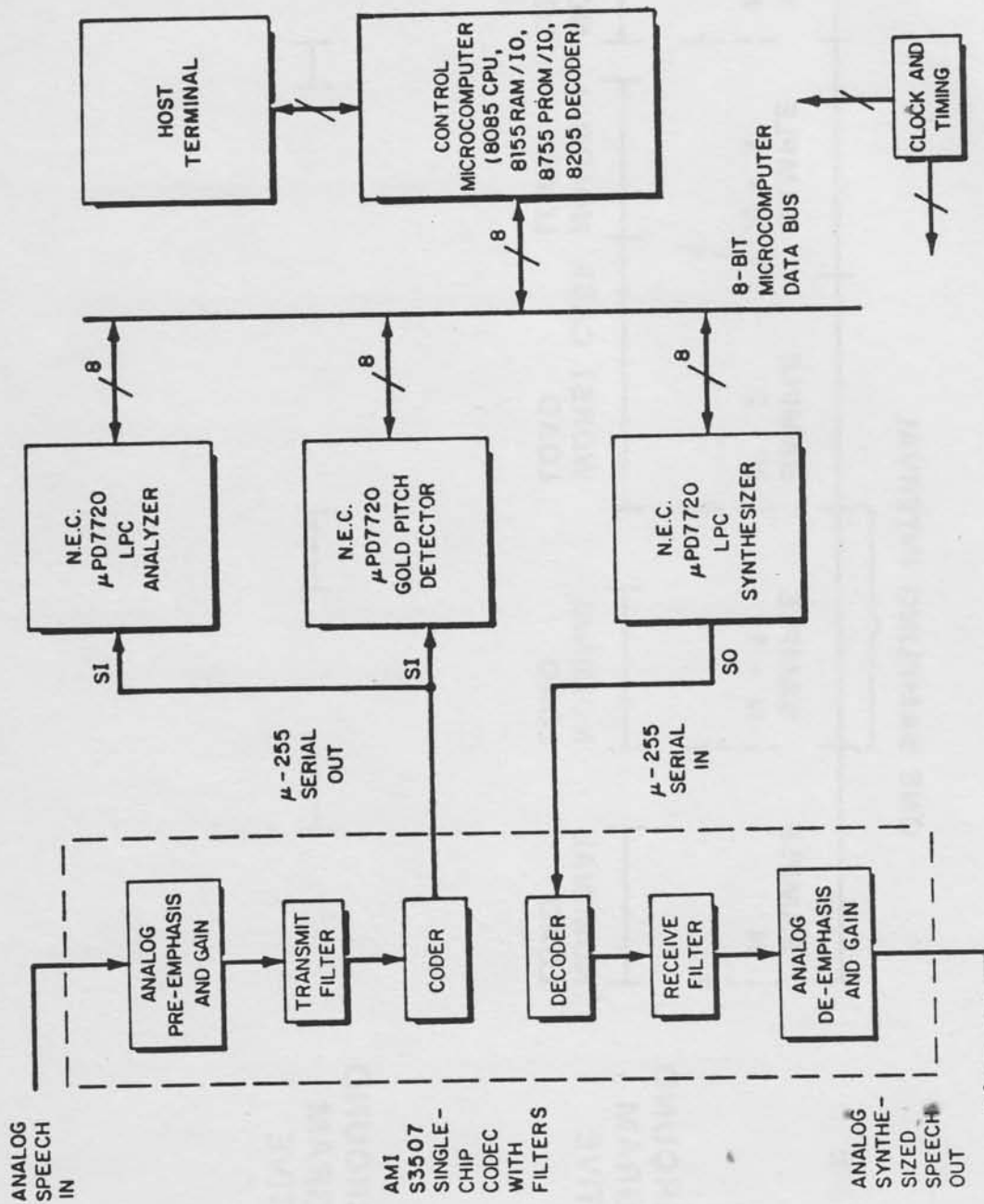


- MULTI-PROCESSOR ARCHITECTURE
- FULLY DIGITAL
- FULL DUPLEX CAPABILITY
- 2.4 kbps TRANSMISSION RATE
- NO CUSTOM LSI

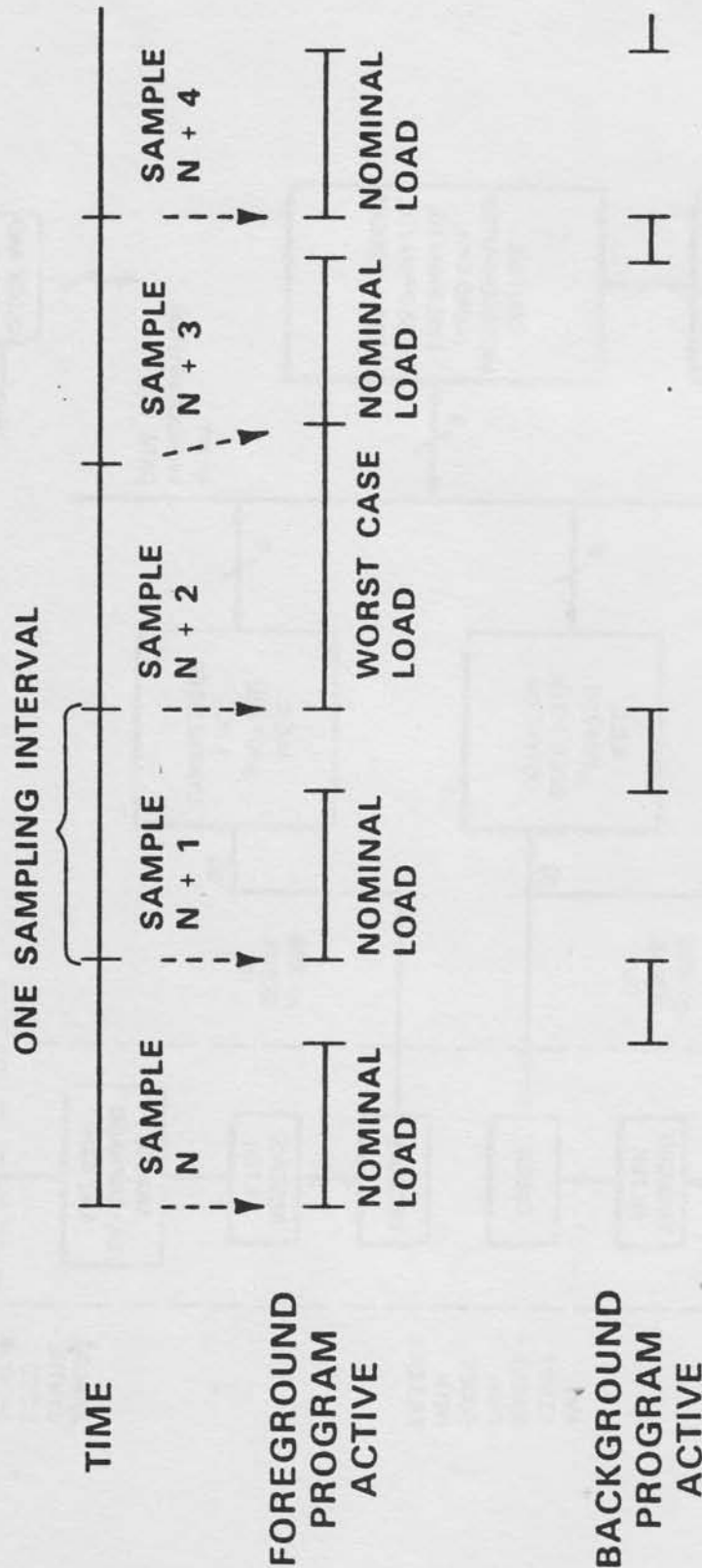
- NMOS LSI TECHNOLOGY
- 5.5 W
- 16 INTEGRATED CIRCUITS
- 18-in.² IC AREA

116381-R





COMPACT VOCODER 'STREAMED' PROGRAM STRUCTURE



LPC ANALYZER TASKS (1 N.E.C. μ PD7720)

- EXECUTED EACH SAMPLE (Interrupt Driven Foreground)
 - (a) INPUT SAMPLE, MU-LAW TO LINEAR CONVERSION, HAMMING WINDOW, DOWNSCALE, UPDATE CORRELATION COEFFICIENTS
 - (b) CHECK FOR FRAME MARK FROM CONTROL PROCESSOR
 - (c) IF FRAME TIME, ACTIVATE BACKGROUND ROUTINE AND SWAP OUTPUT PARAMETER BUFFERS
- EXECUTED EACH FRAME (Background)
 - (a) BLOCK FLOATING POINT CORRELATION COEFFICIENTS AND COMPUTE REFLECTION COEFFICIENTS
 - (b) TRANSFER REFLECTION COEFFICIENTS AND ENERGY ESTIMATE TO CONTROL PROCESSOR



GOLD PITCH DETECTOR TASKS (1 N.E.C. μ PD7720)

- EXECUTED EACH SAMPLE (Interrupt Driven Foreground)
 - (a) INPUT SAMPLE, MU-LAW TO LINEAR CONVERSION, LOW-PASS PRE-FILTER, PEAK-DETECTION, UPDATE SIX PARALLEL PITCH PERIOD ESTIMATES
 - (b) CHECK FOR FRAME MARK FROM CONTROL PROCESSOR
 - (c) IF FRAME TIME, ACTIVATE BACKGROUND ROUTINE
- EXECUTED EACH FRAME (Background)
 - (a) PITCH PERIOD SCORING AND FINAL VOICING DECISION AND PITCH ESTIMATION
 - (b) OUTPUT VOICING DECISION AND PITCH ESTIMATE TO CONTROL PROCESSOR



LPC SYNTHESIZER TASKS (1 N.E.C. μ PD7720)

- EXECUTED EACH SAMPLE (Interrupt Driven Foreground)
 - (a) UPDATE EXCITATION GENERATOR, UPDATE LATTICE FILTER, OUTPUT SAMPLE
 - (b) CHECK FOR FRAME MARK FROM CONTROL PROCESSOR
 - (c) IF FRAME TIME, ACTIVATE BACKGROUND ROUTINE AND SWAP INPUT PARAMETER BUFFERS
- EXECUTED EACH FRAME (Background)
 - (a) CONVERT ENERGY ESTIMATE TO PITCH PULSE AMPLITUDES (Voiced Frames) OR PSEUDO-RANDOM NOISE AMPLITUDES (Unvoiced Frames)
 - (b) INPUT PITCH/VOICING PARAMETER, ENERGY ESTIMATE AND REFLECTION COEFFICIENTS FROM CONTROL PROCESSOR



CONTROL MICROCOMPUTER TASKS (1 INTEL 8085)

- EXECUTED EACH FRAME

(a) GIVE FRAME MARK TO ANALYZER, PITCH DETECTOR AND SYNTHESIZER

(b) INPUT ANALYSIS PARAMETERS FROM ANALYZER AND PITCH DETECTOR, CODE TO 2400 bps, OUTPUT TO HOST TERMINAL

(c) INPUT SYNTHESIS PARAMETERS FROM HOST TERMINAL, DECODE TO 16-bit VALUES, OUTPUT TO SYNTHESIZER



LPC VOCODER MEMORY REQUIREMENTS **(10th Order Model)**

	Percentage of:		
	Data RAM (128 x 16)	Program ROM (512 x 23)	Data ROM (512 x 13)
Gold Pitch Detector	94%	95%	10%
Linear Predictive Analysis	70%	80%	3%
Synthesis	63%	67%	0%

116361-N



LPC VOCODER REAL-TIME USAGE

- (a) 10th ORDER LINEAR PREDICTIVE MODEL
- (b) 8-kHz SAMPLING FREQUENCY
- (c) 22.5-ms SPEECH FRAMES

PERCENTAGE OF REAL-TIME USED

GOLD PITCH DETECTOR	≈35%
LINEAR PREDICTIVE ANALYSIS	63%
SYNTHESIS	46%



CONTROL MICROCOMPUTER REAL-TIME AND MEMORY REQUIREMENTS

- 67% REAL-TIME (22.5 ms Frames, 8 MHz X-TAL)
- 2013 BYTES ROM
- 139 BYTES RAM



COMPACT LPC VOCODER INITIALIZATION OPTIONS

- LINEAR PREDICTIVE MODEL ORDER (up to 15)
- ANALYSIS AND SYNTHESIS FRAME SIZE
- SPEECH SAMPLING FREQUENCY
- SPEECH INPUT/OUTPUT CODING FORMAT
 - (a) 16-bit LINEAR
 - (b) 8-bit MU-255 LAW
- PERFORMANCE OPTIMIZATION FOR INPUT SPEECH BACKGROUND NOISE LEVEL



SUMMARY

- VERY FLEXIBLE, COMPACT LPC VOCODER BASED ON A COMMERCIAL SIGNAL PROCESSING MICROCOMPUTER
- IMPLEMENTATION ACHIEVES ORDER OF MAGNITUDE DECREASE IN
 - (a) POWER DISSIPATION
 - (b) INTEGRATED CIRCUIT AREA
 - (c) PRODUCTION COST
- VOCODER SUCCESSFULLY IMPLEMENTED AND DEMONSTRATED USING EPROM VERSIONS OF THE N.E.C. μ PD7720



FLEXIBLE ARRAY PROCESSORS

GLEN CULLER
CHI SYSTEMS, INC.

DEVELOPMENT OF FLEXIBLE ARRAY PROCESSORS

1. ARRAY PROCESSOR OVERVIEW
2. SIGNAL PROCESSING FRO ARC
3. THE FIRST LPC SPEECH ON ARPANET
4. THE FPS-120B COMMERCIALIZATION
5. THE PLASMA SIMULATION SPINOFF
6. THE LPCAP
7. THE CHI-5, A GENERAL PURPOSE ARRAY PROCESSOR
8. CHI-5 ARCHITECTURE ONTO VLSI CHIPS

CHI-5 CHARACTERISTICS

1. GENERAL PURPOSE COMPUTER WITH ARRAY PROCESSOR INTERIOR
2. TWO ARRAY MEMORIES 1024 WORDS EACH
3. MATRIX ADDRESSING FOR ARRAY MEMORIES
4. FOUR STAGE PROGRAMMABLE PIPELINE
5. 16 PORT MEMORY
 - 8 PROCESS PORTS
 - 8 IO PORTS
6. Q-BUS AND UNIBUS INTERFACES
7. TWO CHANNEL RS-232 INTERFACE

CHI-5 EXECUTION TIMES

DOT PRODUCT: N/4 μ sec

LATTICE REDUCTION: N/2 μ sec

2 MULTIPLIER LATTICE FILTER:
(10 POLE) 9N μ sec

RUNNING AVERAGE: .75N μ sec

FLOATING POINT:

ADD 3 μ sec

MULTIPLY 3 μ sec

DIVIDE 8 μ sec

LOGARITHM 10 μ sec

FFT:

128 COMPLEX 1.24 - 1.5 msec

1024 COMPLEX 11.50 - 15.0 msec

1024 COMPLEX 6.20 - 8.0 msec

LPC (164 POINT FRAME):

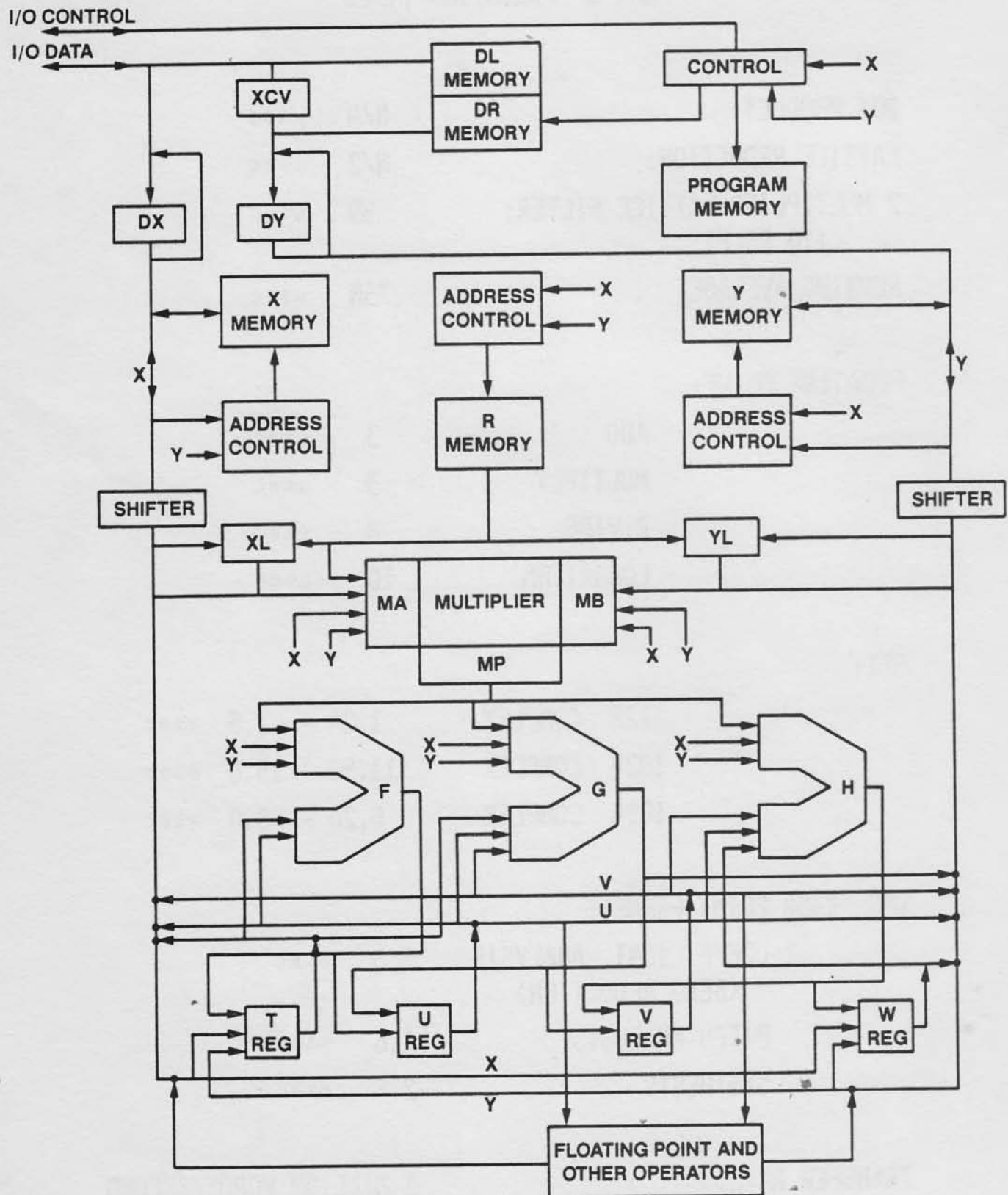
COEFFICIENT ANALYSIS 2.3 msec
(BERG REDUCTION)

PITCH ANALYSIS 1.6 msec

SYNTHESIS 2.5 msec

TRANSFER RATE: 1 MILLION WORDS/SECOND

ARRAY PROCESSOR ARCHITECTURE



VLSI ARRAY PROCESSOR

EDWARD GREENWOOD
MOTOROLA - GOVERNMENT
ELECTRONICS GROUP

PROGRAM OBJECTIVES

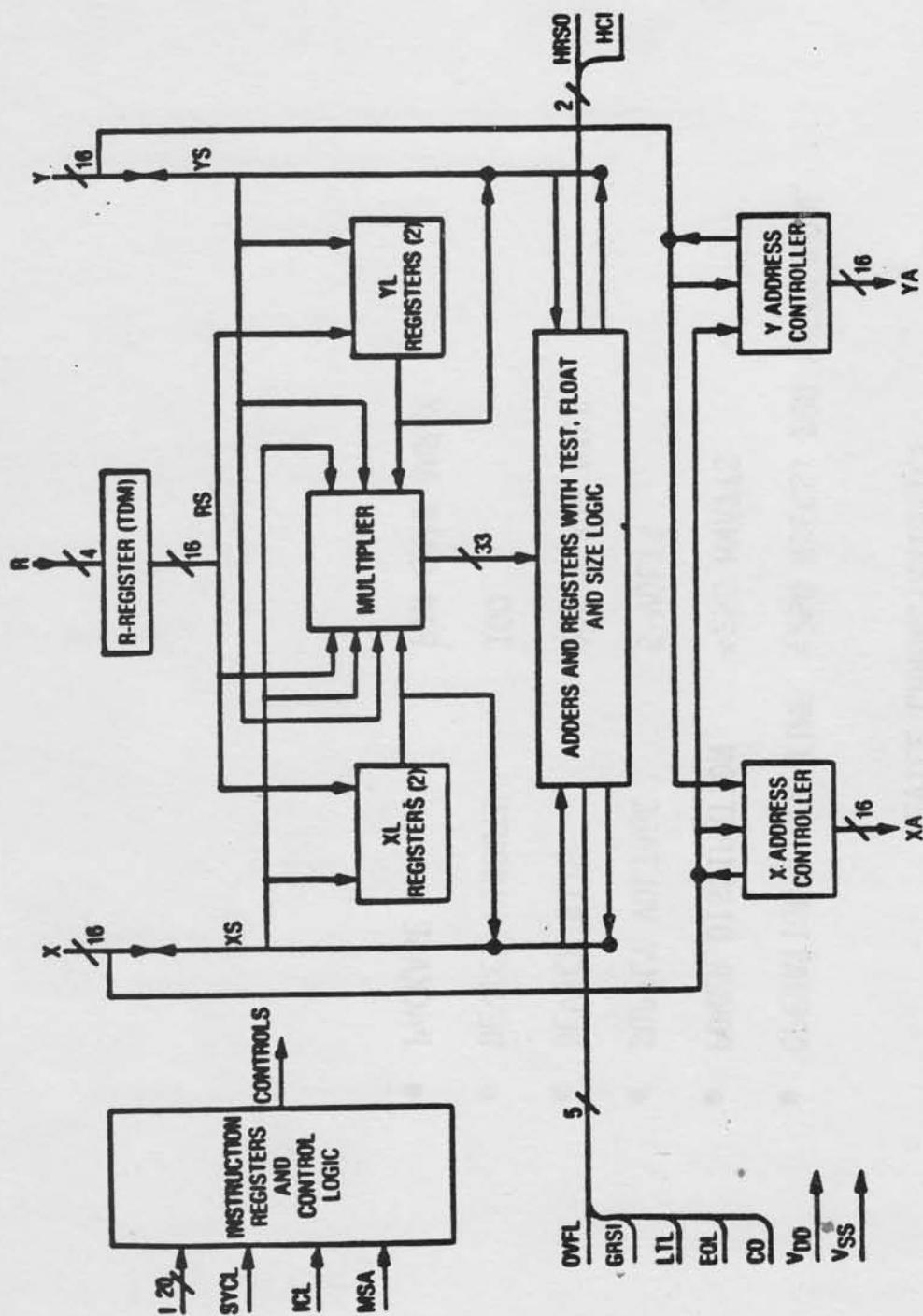
- DELIVER VLSI ARITHMETIC PROCESSOR CHIPS
- DELIVER TWO DEMONSTRATION SYSTEMS
- DEVELOP SINGLE MODULE ARRAY PROCESSOR CONCEPT
- DELIVER SOFTWARE DEVELOPMENT TOOLS
 - TRANSPORTABLE - FORTRAN 77
 - LAYERED - ARITHMETIC PROCESSOR
 - DEMONSTRATION SYSTEM
 - SIMULATORS AND ASSEMBLERS

ALGORITHM EXECUTION TIMES

<u>ALGORITHM</u>	<u>TIME (1)</u>
1024 POINT COMPLEX FFT	5632 μ SECS
512 POINT REAL FFT	1152 μ SECS
1024 POINT REAL VECTOR MULTIPLICATION	260 μ SECS
1024 POINT COMPLEX MULTIPLY	520 μ SECS
DARPA 2400 BIT FULL DUPLEX VOICE PROCESSING	≤ 5263 μ SECS
COMPLEX CONJUGATE POLE-ZERO PAIR FILTER WITH GAIN	1.25 μ SECS/POINT
32 BIT MANTISSA FLOATING POINT ADDITION	1.5 TO 2.5 μ SECS
32 BIT MANTISSA FLOATING POINT MULTIPLICATION	.75, 1.0 OR 1.75 μ SECS
1 MULTIPLICATION AND 3 DATA ADDITIONS	250 NSECS

(1) BASED ON 4 MHZ SYSTEM CLOCK FREQUENCY AND
BLOCK FLOATING POINT ARITHMETIC FOR PROCESSES

ARITHMETIC PROCESSOR UNIT



DEVICE CHARACTERISTICS

- OPERATION CYCLE TIME ≤ 250 NSECS; 200 NSECS GOAL
- POWER DISSIPATION < 250 MWATTS
- SUPPLY VOLTAGE 5 VOLTS
- DEVICE SIZE 298 X 305 MILS
- DEVICE PINOUTS 100
- PACKAGE PIN GRID ARRAY

The diagram illustrates the 305 MILS computer architecture, showing a central processing unit with various functional blocks and a surrounding memory array.

Memory Array:

- Top Memory (X00-X47):** Addresses X00 to X47, with X00-X07 labeled as X00-X07.
- Bottom Memory (Y00-Y47):** Addresses Y00 to Y47, with Y00-Y07 labeled as Y00-Y07.

Central Processing Unit:

- Top Section:** Contains the **INSTRUCTION REGISTER** and **ADDERS AND REGISTERS** block, which includes **REGISTER DECODE FOR ADDERS AND REGISTERS**.
- Middle Section:** Contains the **MULTIPLIER** block, which includes **INSTRUCTION REGISTER DECODE FOR ADD AND SUBTRACT AND MULTIPLIER**.
- Bottom Section:** Contains the **ADDERS AND REGISTERS** block, which includes **REGISTER DECODE FOR ADDERS AND REGISTERS**.

Control and Data Paths:

- Control Logic:** Includes **INSTRUCTION LOGIC FOR XAC** and **INSTRUCTION LOGIC FOR YAC**.
- Data Paths:** Labeled with **LSB** (Least Significant Bit) and **MSB** (Most Significant Bit).
- Buses:** Labeled with **X1 (16)**, **X2 (16)**, **X3 (16)**, **X4 (16)**, **X5 (16)**, **X6 (16)**, **X7 (16)**, **X8 (16)**, **X9 (16)**, **X10 (16)**, **X11 (16)**, **X12 (16)**, **X13 (16)**, **X14 (16)**, **X15 (16)**, **X16 (16)**, **X17 (16)**, **X18 (16)**, **X19 (16)**, **X20 (16)**, **X21 (16)**, **X22 (16)**, **X23 (16)**, **X24 (16)**, **X25 (16)**, **X26 (16)**, **X27 (16)**, **X28 (16)**, **X29 (16)**, **X30 (16)**, **X31 (16)**, **X32 (16)**, **X33 (16)**, **X34 (16)**, **X35 (16)**, **X36 (16)**, **X37 (16)**, **X38 (16)**, **X39 (16)**, **X40 (16)**, **X41 (16)**, **X42 (16)**, **X43 (16)**, **X44 (16)**, **X45 (16)**, **X46 (16)**, **X47 (16)**.

FUTURE ARRAY PROCESSOR MODULE

SIZE - LESS THAN 50 SQUARE INCHES

POWER - LESS THAN 10 WATTS

NUMBER OF TOTAL PARTS* - LESS THAN 30

* WITH THE FOLLOWING MEMORY⁽¹⁾

I/O MEMORY - 8K X 16 RAM

MACRO MEMORY - 1K X 16 PROM

VECTOR SCRATCH MEMORY - 4K X 16 RAM

MICROCODE MEMORY - 2K X 128 PROM

(1) MEMORY SIZES CAN BE EXPANDED

PROGRAM STATUS

- CHIP IN MASK SHOP
- DEMONSTRATION SYSTEM IN TEST
- SOFTWARE TASKS COMPLETED

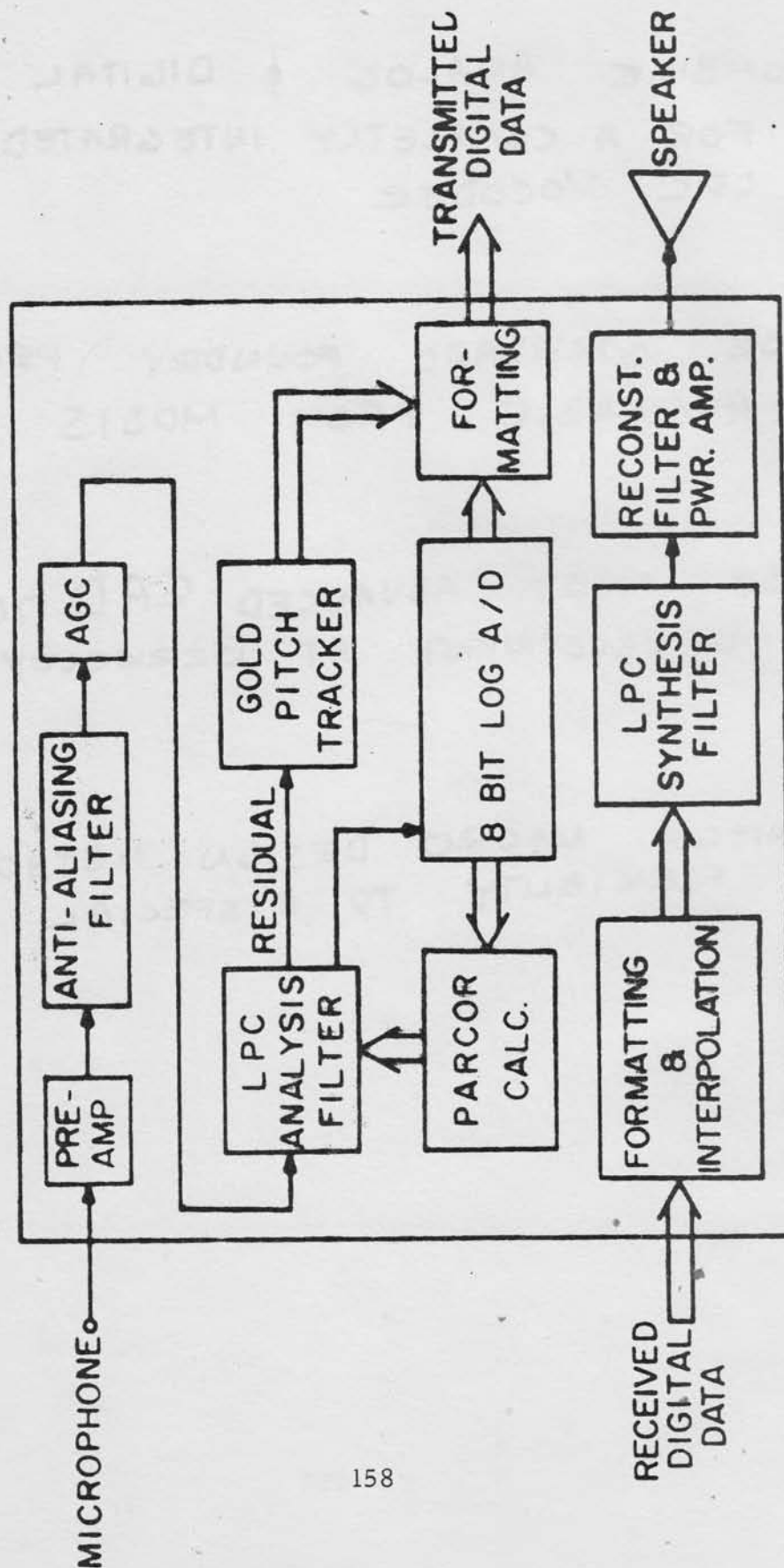
SINGLE CHIP LPC

ROBERT BRODERSEN
UNIV. OF CALIFORNIA/BERKELEY

SINGLE CHIP LPC

- COMBINE ANALOG & DIGITAL FUNCTIONS FOR A COMPLETELY INTEGRATED, FULL DUPLEX LPC VOCODER
- USE STANDARD FOUNDRY PROCESSING AVAILABLE FROM MOSIS
- USE MOST ADVANCED CAD TOOLS UNDER DEVELOPMENT AT BERKELEY
- LARGE MACRO DESIGN METHODOLOGY TO GIVE FLEXIBILITY TO A SPECIAL PURPOSE DESIGN

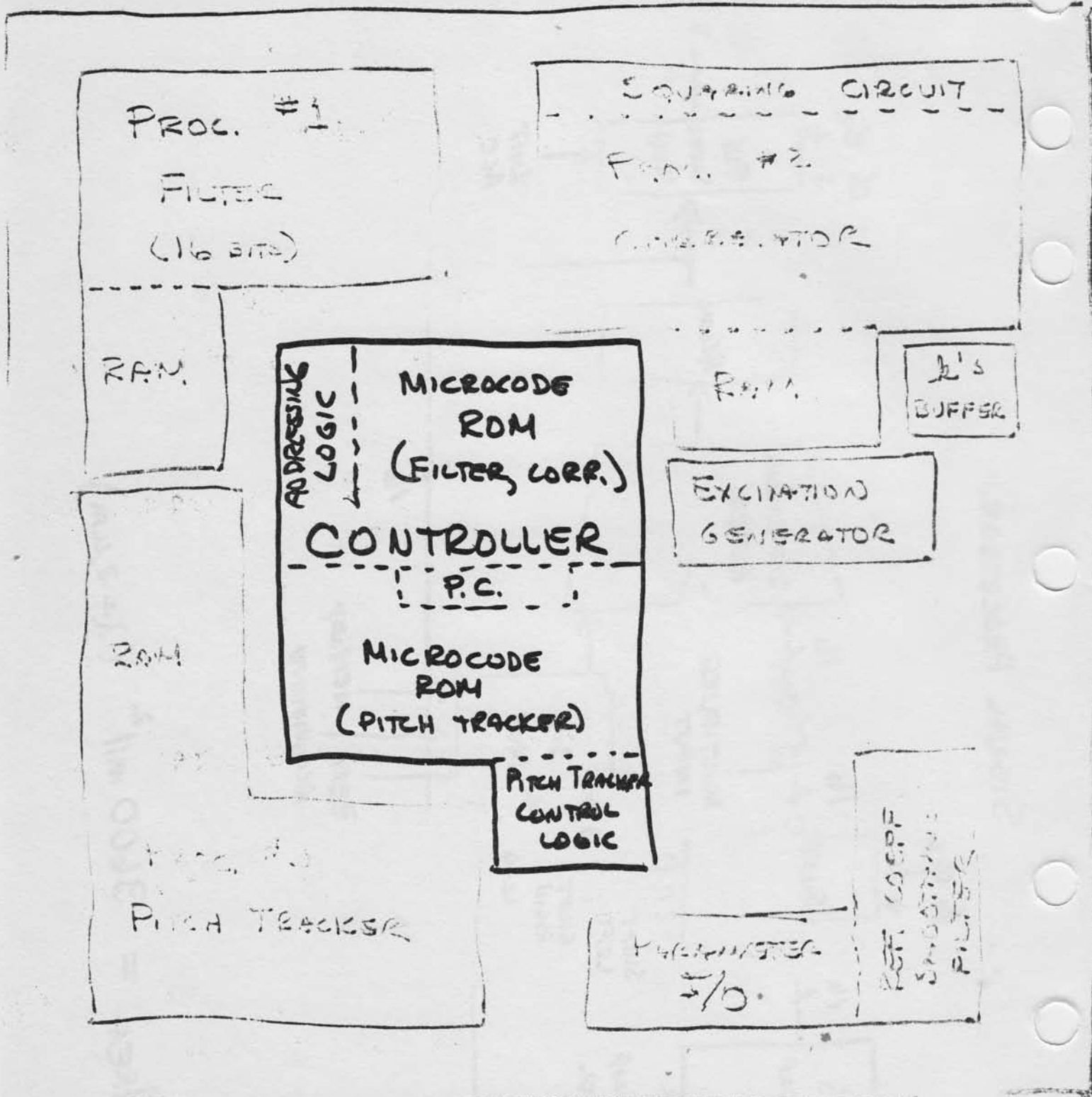
PROPOSED LPC VOCODER CHIP





$$\text{Area} = 3600 \text{ mil}^2 \quad (\lambda = 2 \mu\text{m})$$

CHIP LAYOUT



INCHES

160

PARALLEL PROCESSORS

PROCESSOR 1 : ANALYSIS FILTER,
SYNTHESIS FILTER, PRE-EMPHASIS, DE-EMPHASIS
PITCH TRACKER FILTER

PROCESSOR 2: REFLECTION COEFFICIENT
CALCULATION AND RESIDUAL ENERGY
ESTIMATE

PROCESSOR 3: GOLD-RAGNER ALGORITHM
AND VOICING DECISION

MISC. BLOCKS

EXCITATION GENERATOR: FORMS EXCITATION
WAVEFORM.

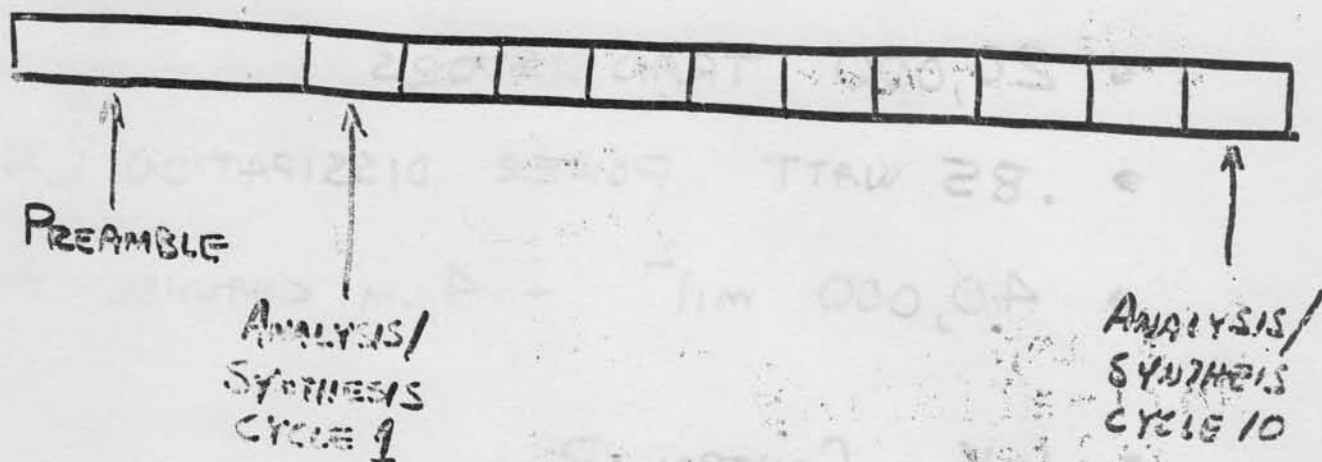
PARAMETER I/O: COMMUNICATES WITH μP

CONTROLLER: PROGRAM COUNTER, MICROCODE ROM,
ADDRESSING ARITHMETIC, GENERATES
ALL CONTROL SIGNALS

LPC Vocoder chip summary

	Area (sq. mils)	Power (milliwatts)
Pre-amp	- 400	5
Anti-aliasing filter	- 2400	8
AGC	- 2000	10
LPC filters (5000)	2x5000 =10,000	2x10 =20
LPC digital correlator (7500)	10,000	40
A/D converter	- 10,000	150
Pitch tracker filters	(10,000) 4200	15
estimators	4800	15
scoring	(7800)	20
Formatting		
Interpolation		
Clocks (2000)	8000	32
Power amp & output filt.-	2000	15
Total	61,600	330

SIGNAL PROCESSOR EXECUTION CYCLE



PREAMBLE : PRE-EMPHASIS, DE-EMPHASIS AND LOW PASS FILTER FOR PITCH TRACKER; NOMINALLY 32 INSTRUCTIONS

ANALYSIS/
SYNTHESIS : 10 CYCLES OF 32 INSTRUCTIONS
= 320 ; 16 INSTRUCTIONS FOR EACH FILTER

CLK. RATE = $352 \times 8 \text{ kHz} = 2.816 \text{ MHz}$

SUMMARY

- 20,000 TRANSISTORS
- .85 WATT POWER DISSIPATION (NMOS)
- 40,000 mil^2 - 4 μm CHANNEL LENGTH
- 6K CONTROL ROM
- 2K DYNAMIC RAM
- 3 PARALLEL PROCESSORS